Dear Reader,

Two years ago, we expanded our portfolio of chemicals for micro-structuring to include silicon wafers. A steadily growing network of wafer manufacturers and service providers allows us to fulfil special wafer requests as well as to offer big volume prices even to our customers with small and medium demand.

Therefore, we decided this was a perfect opportunity to create this brochure containing technical information related to silicon wafers.

With the help of illustrations we would like to show the way from quartz sand to finished and structured silicon wafers, how wafers are specified and the assortment we can offer.

Wishing you much success!

Your MicroChemicals Team
**From Quartz to High-Purity Silicon**

**Silicon in the Universe and on Earth**

Hydrogen and helium dominate the visible matter of the universe, the mass fraction of silicon is less than 0.1 %. This element mainly arises from the fusion of two oxygen nuclei ($2^{16}$O ‡ $^{28}$Si + $^4$He) at temperatures $> 10^9$ K inside stars with more than eight solar masses.

The entire planet Earth contains approx. 17 % silicon, the third most abundant element after iron and oxygen, closely followed by magnesium.

In the earth’s iron-based core, silicon (= 7 mass %) is the second most abundant element.

The earth’s approx. 40 km thick crust contains silicon (in the form of silicates and SiO$_2$) with a mass fraction of 28 % as the second most abundant element after oxygen. Quartz = crystalline SiO$_2$ is the raw material for silicon production.

**Metallurgical-Grade Silicon Production**

Quartz sand is reduced with carbon in an electric arc furnace at temperatures $> 1900^\circ$C to metallurgical grade silicon ($> 98 $ % pure). The major part of the world production (2008: approx. 6 million tons) is used for manufacturing alloys with aluminium and steel, and as raw material for polysiloxane production.

In 2010, Si wafer production consumed approx. 200 kilotons purified silicon. Approx. 90 % of this volume was used for mono- and polycrystalline solar cells, the remaining 10 % (corresponding to a wafer area of $\approx 5$ km$^2$) went into the semiconductor industry.

**Purification of Silicon**

The impurity concentration in metallurgical-grade silicon is many orders of magnitude too high for an application in photovoltaics and microelectronics, thus the silicon has to be purified.

For this reason, silicon intended for wafer production is converted into trichlorosilane gas (HSiCl$_3$) at $= 300^\circ$C using hydrochloric acid via

$$ Si + 3 \text{HCl} \rightarrow \text{HSiCl}_3 + \text{H}_2 $$

which already removes many impurities which don’t form volatile chlorine compounds at the applied process temperature.

Trichlorosilane (boiling point 32°C) mixed with other gaseous chlorine compounds undergoes multiple distillation thereby improving the purity up to 99,9999999 %. („9N“) and is subsequently thermally decomposed to polycrystalline silicon.
The polycrystalline silicon formation is performed in the so-called Siemens-Process (fig. left): The purified trichlorosilane mixed in hydrogen is thermally decomposed on the surface of a heated (approx. 1100°C) silicon rod via

$$\text{HSiCl}_3 + \text{H}_2 \xrightarrow{\text{â}} \text{Si} + 3 \text{HCl}\]

to polycrystalline silicon and HCl, which corresponds to the reverse reaction of the trichlorosilane formation.

This "electronic-grade" (purity concentration < $10^{14}$ cm$^{-3}$) polysilicon is the raw material for silicon single crystals which are grown by two different processes as described in the following sections.

**Growth Techniques for Monocrystalline Silicon Ingots**

**Czochralski-Technique**

**Basics**

The Czochralski-technique is a method to pull a monocrystal with the same crystallographic orientation of a small monocrystalline seed crystal out of melted silicon.

First, electronic-grade polysilicon nuggets (e. g. from the Siemens-process) optionally together with dopants are melted in a quartz crucible at a temperature > 1400°C in an inert gas atmosphere (e. g. argon). The quartz crucible sits inside a graphite container which – due to its high heat conductivity – homogeneously transfers the heat from the surrounding heater to the quartz crucible.

The silicon melt temperature is kept constant roughly above the silicon melting point. A monocrystalline silicon seed crystal with the desired crystal orientation (e. g. <100>, <110> or <111>) is immersed into the melt and acts as a starting point for the crystal formation supported by the heat transfer from the melt to the already grown crystal.

The seed crystal is slowly (few cm/hour) pulled out of the melt, where the pull speed determines the crystal diameter. During crystal growth, the crystal as well as the crucible counter-rotate in order to improve the homogeneity of the crystal and its dopant concentration.

Before the crystal growth is finished, a continuous increase of the pull speed reduces the crystal diameter towards zero. This helps prevent thermal stress in the ingot which could happen by an abrupt lifting out of the melt and could destroy the crystal.

**Advantages and Disadvantages**

The Czochralski-technique allows big crystal diameters (state of the art: 18 inch = 46 cm) and – compared to the float-zone technique described in the following section – lower production cost per wafer.

One disadvantage of the Czochralski-technique is impurities such as oxygen (typ.
$10^{18}\text{ cm}^{-3}$) and carbon (typ. $10^{17}\text{ cm}^{-3}$) from the quartz and graphite crucible which lower the minority carrier diffusion length in the finished silicon wafer.

Another disadvantage is a comparably low homogeneity of the axial and radial dopant concentration in the crystal caused by oscillations in the melt during crystal growth. This makes it difficult to attain high-ohmic CZ-wafers with a resistivity exceeding $\approx 100\text{ Ohm cm}$). A magnetic field (“Magnetic Czochralski”, MCZ) can retard these oscillations and improve the dopant homogeneity in the ingot.

The different process steps of Czochralski crystal growth: Melting of polysilicon with dopants, immersion of the seed crystal, crystal growth.
**Float-Zone Technique**

A monocrystalline silicon seed crystal is brought into contact with one end of a polycrystalline silicon ingot. Starting from here, an RF coil melts a small region of the polysilicon which, after cooling down, forms monocrystalline silicon with the crystallographic orientation of the seed crystal (e.g. <100>, <110> or <111>).

The RF coil and the melted zone move along the entire ingot. Since most impurities are less soluble in the crystal than in the melted silicon, the molten zone carries the impurities away with it. The impurities concentrate near the end of the crystal where finally they can simply be cut away. This procedure can be repeated one or more times in order to further reduce the remaining impurity concentration.

Doping is realized during crystal growth by adding dopant gases such as phosphine (PH$_3$), arsine (AsH$_3$) or diborane (B$_2$H$_6$) to the inert gas atmosphere.

**Advantages and Disadvantages**

The main advantage of the float-zone technique is the very low impurity concentration in the silicon crystal. In particular the oxygen and carbon concentration are much lower as compared to CZ silicon, since the melt does not come into contact with a quartz crucible, and no hot graphite container is used.

Additionally, the dopant concentration in the final crystal is rather homogeneous and manageable which allows very high-ohmic (1 - 10 KOhm cm) wafers as well as wafers with a narrow specified electrical resistivity.

However, FZ silicon is more expensive than CZ silicon, and the crystal diameter is limited to eight inches (state of the art).
From Single Crystals to Polished Wafers

**Grinding**

The ingots grown with the Czochralski or float-zone technique are ground to the desired diameter and cut into shorter workable cylinders with e. g. a band saw and ground to a certain diameter.

An orientation flat is added to indicate the crystal orientation (schema right), while wafers with an 8 inch diameter and above use a single notch to convey wafer orientation, independent from the doping type.

**Dicing**

Two common techniques are applied for wafer dicing: Inside hole saw and wire saw, both explained in the following sections.

**Inside Hole Saw (Annular Saw)**

The wafers are sawed inside a circular blade whose cutting edge is filled with diamond splinters (schema right).

After sawing, the wafer surfaces are already relatively flat and smooth, so the subsequent lapping of the surfaces takes less time and effort.

However, only one wafer per annular saw can be cut at the same time, so this technique has a comparably low throughput which makes the wafers more expensive compared to wafers cut by a wire saw.

**Wire Saw**

In order to increase throughput, wire saws with many parallel wires are used which cut many
A long (up to 100 km) high-grade steel wire with a diameter of ≈ 100 - 200 µm is wrapped around rotating rollers with hundreds of equidistant grooves at a speed of typically 10 m/s. The mounted silicon cylinder is drained into the wire grid and thus cut into single wafers.

The wire is either coated with diamond splinters or wetted with a suspension of abrasive particles such as diamonds or silicon carbide grains, and a carrier (glycol or oil). The main advantage of this sawing method is that hundreds of wafers can be cut at a time with one wire. However, the attained wafer surface is less smooth and more bumpy as compared to wafers cut by an annular saw, so the subsequent lapping takes more time.

**Lapping**

After dicing, the wafers are lapped on both sides in order to i) remove the surface silicon which has been cracked or otherwise damaged by the slicing process (e. g. grooves by the wire saw) and ii) thinned to the desired wafer thickness.
Several wafers at a time are lapped in between two counter-rotating pads by a slurry consisting of e. g. Al₂O₃ or SiC abrasive grains with a defined size distribution.

**Etching**
Wafer dicing and lapping degrade the silicon surface crystal structure, so subsequently the wafers are etched in either KOH- or HNO₃/HF based etchants in order to remove the damaged surface.

**Polishing**
After etching, both wafer surfaces appear like the rear side of finished single-side polished wafer. In order to attain the super-flat, mirrored surface with a remaining roughness on atomic scale, the wafers have to be polished.
Wafer polishing is a multi-step process using an ultra-fine slurry with 10 - 100 nm sized grains consisting of e. g. Al₂O₃, SiO₂ or CeO₂ which, combined with pressure, erode and mechanically and chemically smoothen the wafer surface between two rotating pads.

**Cleaning**
Finally, the wafers are cleaned with ultra-pure chemicals in order to remove the polishing agents thereby making them residual-free.
Further Process Steps

**Thermal Oxidation of Silicon**

**Fields of Application**

The electronic (resistivity $10^{14} \ldots 10^{16}$ Ohm·cm, breakthrough field $10^6 \ldots 10^7$ V/cm, barrier for electrons and holes from crystalline Si > 3 eV), mechanical (melting point approx. 1700°C) and optical (transparent in the visible as well as near infrared and ultraviolet spectral range) properties of SiO₂ make it a suitable material for the dielectric film in transistors, capacitors (DRAM) or flash-memories; and as a hard mask for diffusion, implantation, wet or dry chemical etching; and generally as an isolator between integrated devices, or as an antireflection layer on e. g. solar cells.

Required SiO₂ film thicknesses range from a few nm (gate-oxide of state-of-the-art CMOS transistors) up to several µm for electrical insulation. Compared to sputtered or CVD SiO₂, thermal SiO₂ reveals a better and more reproducible electrical insulation.

**Oxidation Technique**

Compared to (crystalline) quartz, native (= few nm grown at room temperature in air) and thermal (growth temperature 800 - 1200°C) silicon dioxide (schema of an oxidation furnace right) is amorphous (= without long-term atomic lattice order). The silicon in native or thermally grown SiO₂ evolves from the Si substrate, which is partially consumed during SiO₂ growth: 100 nm SiO₂ requires approx. 46 nm Si, while the wafer thickness simultaneously increases by approx. 54 nm.

One has to distinguish between dry oxide (Si + O₂ $\rightarrow$ SiO₂), and – with H₂O as process gas – wet oxide (Si + 2 H₂O $\rightarrow$ SiO₂ + 2 H₂).

At the same process parameters, due to the higher growth rate, wet oxide reveals a higher porosity and HF etch rate.
Oxidation Rate and Attainable SiO₂ Film Thickness

At the beginning of thermal SiO₂ growth, the chemical reactions on the surface/interface limit the film thickness which increases linearly with time.

With the SiO₂ thickness increasing, the more and more dominating oxygen diffusion through the already-grown film towards the Si/SiO₂-interface limits the growth rate. The SiO₂ thickness now increases with the square-root of growth time.

Besides the process gas composition (O₂/H₂O), their partial pressure as well as the substrate temperature (activation energy of oxygen diffusion and chemical reaction at the Si/SiO₂-interface), the SiO₂ growth rate also depends on the Si substrate crystal orientation, mechanical strain of the substrate (e. g. in case of already processed device layers), as well as on substrate doping (e. g. faster oxide growth on phosphorus doped silicon).

Silicon Nitride Coating

In the field of tool-making, stoichiometric trisilicon tetranitride (Si₃N₄) with its very high mechanical and thermal stability is used for tools such as roller bearings used under harsh conditions.

For semiconductor devices, the chemical, electrical and optical properties of amorphous hydrogenated silicon nitride (SiNx) make this material well-suited for different applications, such as for

- passivation or insulating layers in integrated circuits
- masking or etch stop material in wet and plasma etching processes due to its high chemical stability
- masking material in silicon oxidation processes due to the very low oxygen diffusion coefficient in SiNₓ
- anti-reflective coating in photovoltaics due to its adjustable refractive index

SiNx layers realized by the chemical vapour deposition (CVD) technique from SiH₄ and NH₃ typically – depending on the deposition temperature and gas composition – contain 5 - 20 atom% hydrogen which saturates dangling bonds and thus chemically and mechanically stabilizes the SiNₓ lattice.

SiNx can be etched via photoresist masks either with buffered or unbuffered HF or (selectively to SiO₂) with concentrated phosphoric acid. The HF etch rate of SiNx depends on the SiNx deposition temperature and its refractive index. A hydrogen-rich SiNx film deposited at 100°C with a refractive index of n = 1.9 shows an etch rate of several 100 nm/min in buffered HF (12.5 % HF). The etch rate drops to less than 10 nm/min for SiNx films deposited at 400°C with a refractive index of n = 2.

Properties of Amorphous SiO₂ and SiNx Films

The table below lists “typical” values for selected amorphous SiO₂ and SiNx film properties. Dependant on the deposition conditions, measured values can deviate from these values.

<table>
<thead>
<tr>
<th></th>
<th>Density (g/cm³)</th>
<th>Refractive index @ 400 - 800 nm</th>
<th>BOE 7:1 etch rate 12.5 % HF, 21°C (nm/min)</th>
<th>KOH etch rate 44 %, 80°C (nm/min)</th>
<th>Dielectric strength (kV/cm @ 20°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>2.2</td>
<td>1.4 - 1.5</td>
<td>50 - 100</td>
<td>5 - 10</td>
<td>250 - 400</td>
</tr>
<tr>
<td>SiNx</td>
<td>2.5 - 3.1</td>
<td>1.9 - 2.1</td>
<td>10 - 100</td>
<td>&lt; 1</td>
<td>&gt; 1000</td>
</tr>
</tbody>
</table>
Silicon Epitaxy

Mechanism

In wafer fabrication, silicon epitaxy refers to the growth of a thin layer of single-crystalline silicon onto a single-crystalline silicon substrate, usually via chemical vapour deposition.

Commonly used process gases are silicon tetrachloride (SiCl₂), trichlorosilane (SiHCl₃), dichlorosilane (SiH₂Cl₂) or silane (SiH₄), mixed with hydrogen, which are thermally decomposed to silicon on the surface of wafers heated up to typically 600 - 1000°C. The Si atoms released from the gaseous compounds form crystalline silicon monolayer by monolayer on the silicon substrate.

Fields of Application

The addition of dopants such as phosphine, arsine or diborane to the process gas allows the realization of certain doping profiles in the epitaxial film which is required for e. g. box-shaped doped structures or a low-doped layer on top of highly doped silicon which can not be realized by diffusion.

Already realized films such as areas doped via ion implantation, or microelectronic devices can be buried under an epitaxial layer.

Since the oxygen and carbon concentrations in epitaxial layers are very low, the electronic quality of this film is better than for the silicon substrate underneath, which can be important for integrated devices.

SOI-Wafers

Basics

"Silicon on Insulator"-wafers are wafers with a crystalline silicon film or devices lithographically made from this film located on an electrical insulator such as SiO₂. There are two main fields of application for SOI wafers:

Fields of Application

Transistors located on an electrically insulating film have a lower capacity and smaller electrical current leakage as compared to transistors directly sitting on the silicon substrate. Therefore, the transistors can be packed more densely, their energy consumption is lower, and the switching speed increased which allows higher clock rates and lower power demand.

In micro-optics, the insulating film allows integrated optical components including waveguides in which μm-waves can be guided in silicon (refractive index = 3.5) embedded in SiO₂ (refractive index = 1.5) by total reflection.

Realization

One technique for producing SOI wafers is the SIMOX™-process (Separation by Impiantation of OXygen, see schema right) starting with oxygen implantation in silicon wafers, which allows an accurate control of the depth profile of the implanted O-atoms.

Subsequently, a high temperature step forms the SiO₂ layer where the O-atoms have been captured in the silicon lattice, and thermally anneals the crystal structure of the silicon beyond distorted by the implantation process.

The Smart-Cut™-technique (top of next page) combines hydrogen ion implantation and wafer bonding. Hydrogen ions are implanted in an oxidized silicon wafer. This wafer is bonded with another wafer without SiO₂ layer. A baking step (> 500°C) splits the oxidized wafer along the depth of the implanted hydrogen atoms induced by mechanical stress.
Silicon Wafer Specifications

Diameter, Orientation and Surface

Diameter
The wafer diameter is specified in mm or – most commonly – an integer number of inches (one inch = 25.4 mm) and the diameter tolerance (typ. < 1 mm).

Orientation
The wafer orientation (e.g. <100>, <110> or <111>) denotes the crystallographic plane parallel to the wafer surface. The tilt angle defines the maximum extent to which the wafer surface and crystallographic plane are inclined to each other.

Surface
Usually both sides of silicon wafers are at least lapped and etched. Surface polishing is performed either on one (SSP = Single-Side Polished) or both sides (DSP = Double-Side Polished).

Doping and Resistivity
The dopant atoms incorporated during silicon crystal growth increase the electrical conductivity via an increase in the free electron (in the case of phosphor or arsenic dopants) or hole (boron as dopant) concentration by up to many orders of magnitude beyond the value of undoped silicon.

Below a doping concentration of approx. \(c = 10^{16}\) cm\(^{-3}\) the resistivity drops recipro-\(cally\) with \(c\), towards a higher doping concentration the free carrier mobility drops which flattens the \(R(c)\) dependency (see plot below).

Since the doping concentration is not perfectly homogeneous but axially and radially varies in the silicon crystal, the wafers are specified to a certain range (for CZ wafers typically one order of magnitude, such as 1 - 10 ohm cm, for FZ wafers often more narrow) in the electrical resistivity.

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The dependency of the electrical resistivity from the doping concentration of boron and phosphor / arsenic in crystalline silicon

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fax: +49 (0) 731 977343 29
The crystal structure of silicon with the high stability of the \{111\}-surfaces allows the realisation of pyramids and trenches via anisotropically etching of different orientated substrates.
**Thickness, Thickness Variation and Surface**

The **thickness** usually measured in the centre of a wafer gives no information on how strong the shape of the wafer deviates from an ideal (very flat) cylinder.

**TTV**

The Total Thickness Variation TTV specifies the difference $d_1 - d_2$ (left) between the minimum and maximum thickness of a wafer measured at typically five different locations.

**Bow**

The bow is defined by $d_3 + d_4$ (left) corresponding to the maximum deviation of the median surface to a reference plane.

**Warp**

The value $d_5 + d_6$ (left) corresponds to the deviation of the median surface of the wafer from a reference plane which is already corrected by the bow of the entire wafer.

**Micro-Roughness**

The Root Mean Square ("RMS") denotes the standard height deviation of a surface scan on a wafer.

The RMS values are typically < 1 nm which corresponds to a smoothness on atomic scale!
Wet Etching of Silicon and SiO₂

Anisotropic Silicon Etching

Strong alkaline substances (pH > 12) such as aqueous KOH, NaOH or TMAH solutions, etch silicon via Si + 4 OH⁻ ⇌ Si(OH)₄ + 4 e⁻.

Since the bonding energy of Si atoms is different for each crystal plane and KOH/TMAH Si etching is not diffusion- but etch rate limited, the Si etching is highly anisotropic: While the (100)- and (110)-crystal planes are being etched, the stable {111} planes act as an etch stop allowing interesting applications (illustrated on page 18):

(111)-Wafers are almost never attacked by the etch.
(100)-Wafers form square-based pyramids with {111} surfaces. These pyramids are realised on c-Si solar cells for the purpose of reflection minimization.
(110)-Wafers form perpendicular trenches with {111} sidewalls, used as e. g. micro-channels in micromechanics and microfluidics.

The degree of anisotropy (= etch rate selectivity between different crystal planes), the etch rates and etching homogeneity (plots and figures on page 20 - 24) depend on the etching temperature, atomic defects in the silicon crystal, intrinsic impurities of the Si crystal, impurities (metal ions) by the etchant and the concentration of Si-atoms already etched.

The doping concentration of the Si to be etched also has a strong impact on the etching: During etching, Boron doped Si forms borosilicate glass on the surface which acts as an etch stop if the boron doping concentration exceeds 10¹⁹ cm⁻³.

We supply 44 % KOH as well as 25 % TMAH in VLSI-quality in 2.5 L sales units.

The following two pages show plots depicting the temperature- and concentration-depndent etch rates of (100)- and (110)-Si in KOH and TMAH, as well as the selectivity to SiO₂ which is commonly used as etch mask.

![Graph of (100) : (111) - Selectivity](image-url)
The etch rate of (100)- and (110)-Silicon surfaces in KOH as a function of the KOH concentration and temperature. The alkaline etching of Si requires OH- ions as well as free water molecules. Thus the etch rate (as well as the surface roughness) drops towards higher concentrations.

The (100)-Si : SiO₂ etch rate selectivity in KOH as a function of the KOH-concentration and temperature.
The (100)-Si : SiO$_2$ etch rate selectivity in KOH as a function of the KOH-concentration and temperature.

The (100)-Si : SiO$_2$ etch rate selectivity in TMAH as a function of the TMAH-concentration and temperature. The Si and SiO$_2$ etch rates in TMAH have their maxima at different temperatures, so their ratio shows an S-shape.
**Isotropic Etching of Silicon with HF/HNO$_3$**

**Etch Mechanism**

The following chemical reactions summarize the basic etch mechanism for isotropic silicon etching (steps 1 - 4) and SiO$_2$ (only step 4) using a HF/HNO$_3$ etching mixture:

1. NO$_2$ formation (HNO$_2$ always in traces in HNO$_3$):
   \[
   \text{HNO}_2 + \text{HNO}_3 \rightarrow 2 \text{NO}_2 + \text{H}_2\text{O}
   \]

2. Oxidation of silicon by NO$_2$:
   \[
   2 \text{NO}_2 + \text{Si} \rightarrow \text{Si}^{2+} + 2 \text{NO}_2^- + \text{H}_2\text{O}
   \]

3. Formation of SiO$_2$:
   \[
   \text{Si}^{2+} + 2 (\text{OH})^- \rightarrow \text{SiO}_2 + \text{H}_2\text{O}
   \]

4. Etching of SiO$_2$:
   \[
   \text{SiO}_2 + 6 \text{HF} \rightarrow \text{H}_2\text{SiF}_6 + 2 \text{H}_2\text{O}
   \]

In conclusion, HNO$_3$ oxidises Si, and HF etches the SiO$_2$ formed.

**Silicon Etch Rate**

The plot right shows the etch rate of crystalline Si for different HF : HNO$_3$ mixtures.

The etch rate drops towards zero when either the HF or HNO$_3$ concentration becomes very low, since in pure HF no SiO$_2$ forms which can be etched in HF, and HNO$_3$ only oxidizes the Si without etching it.

An accurate control of the etch rate requires a temperature range within ± 0.5°C. A dilution with acetic acid improves the wetting of the hydrophobic Si-surface and thus increases and homogenizes the etch rate.

Doped (n- and p-type) silicon as well as phosphorus-doped SiO$_2$ etches faster than undoped Si or SiO$_2$.

**Si : SiO$_2$ Etch Selectivity**

As the etch triangle (Fig. right) shows, high HF : HNO$_3$ ratios promote rate-limited etching (strong temperature dependency of the etch rate) of Si via the oxidation (1) - (3), while low HF : HNO$_3$ ratios promote diffusion-limited etching (lower temperature dependency of the etch rate) via step (4). HNO$_3$-free HF etches do not attack Si.

The SiO$_2$ etch rate is determined by the HF-concentration, since the oxidation (1) - (3)
does not apply. Compared to thermal oxide, deposited (e. g. CVD) SiO$_2$ has a higher etch rate due to its porosity; wet oxide a slightly higher etch rate than dry (thermal) oxide for the same reason.

**Isotropic Etching of SiO$_2$ with HF or BHF**

Hydrofluoric acid is the one and only chemical able to isotropically etch SiO$_2$. Due to the high toxicity of concentrated HF, one has to consider the maximum concentration that is really required. 1 % HF is sufficient for removing native SiO$_2$ in a so-called “HF-Dip”, and even 200 - 300 nm oxide can be etched in 10 % HF or buffered HF in a reasonable amount of time. We supply 1 %, 10 %, 50 % HF and buffered HF (BOE 7 : 1 = AF 87.5 - 12.5) in VLSI-quality.

The SiO$_2$ etch rate in buffered HF (BOE) as a function of the ammonia : HF concentration

**Unbuffered and Buffered Hydrofluoric Acid**

Etching of Si and SiO$_2$ with HF consumes F$^-$-ions via the reaction

$$\text{SiO}_2 + 4 \text{HF} \rightarrow \text{SiF}_4 + 2 \text{H}_2\text{O}$$

HF buffered with ammonia fluoride (NH$_4$F + H$_2$O + HF = ‘BHF’) maintains the free F$^-$-ion concentration via NH$_4$F $\rightarrow$ HF + NH$_3$, allowing

+ a constant and controllable etch rate as well as spatial homogeneous etching
+ an increase in the etch rate (factor 1.5 - 5.0) by highly reactive HF$_2^-$-ions and
+ an increase of the pH-value (†) minor resist underetching and resist lifting.

Despite the increased reactivity, strongly buffered hydrofluoric acid has a pH-value of close to seven and therefore may not be detected by chemical indicators!
Diced or Metallized Silicon-, Quartz-, Glass- or Fused Silica Wafers

Wafer Dicing
Wafer dicing allows to cut rectangular pieces from circular wafers. Dicing can be accomplished by scribing and breaking, by mechanical sawing (using a blade or wire saw), or by laser cutting. As the following section shows, almost any parameters are possible. Whether there is a minimum order quantity for your individual request or not: Please feel free to contact us!

Realizable Parameters for Diced Wafer Pieces
Material: CZ-Si or FZ-Si, optionally with thermal SiO₂
Dimensions: From 5 x 5 mm to 120 x 100 mm
Thickness: 200 µm - 10 mm
Orientation: <100> or <111>; <110> on request

Realizable Parameters for Diced Quartz, Glass- and Fused Silica Wafers
Material: Glass, Fused Silica: JGS1, JGS2 and JGS3
Dimensions: From 2 x 2 mm to 300 x 300 mm
Thickness: 100 µm - 10 mm
Orientation: Quartz: ST-, AT-, X-, Y- and Z-Cut

Price for Diced Wafer Pieces
Please ask us for a quote, we will be glad to offer!

Metallization
One or more metal films coated on wafers by either sputtering or thermal evaporation.

Realizable Parameters for Metallized Wafers
Substrate: Silicon (with or without SiO₂), Glass, Quartz, or Fused Silica
Metals: Cu, Ni, Al, Ag, Ti, Au, Pt, Pd ...
Technique: Sputtering or evaporation
Purity: Standard (4N = 99.99 %) or high-purity (6N = 99.9999 %)

Price for Metallization
Cost factors for metallized wafers are the wafers itself, the thickness(es) and purity of the metal film(s), as well as the wafer diameter, the required homogeneity, and the number of wafers.
Please feel free to contact us for a quote!
Our Silicon Wafers

Available Specifications

Growth Method: Czochralski (CZ) and float-zone (FZ)
Diameter: 2, 3, 4, 5, 6 and 8 inch
Thickness: Standard wafer thicknesses are 280 µm (2”), 380 µm (3”), 525 µm (4”), 675 µm (6”) and 725 µm (8”). Thinner wafers (depending on the diameter from approx. 250 µm on) and thicker wafers (mm or cm) on request
Orientation: (100) and (111), (110) on request
Doping: Boron, phosphor and arsenic / intrinsic
El. conductivity: CZ-wafers from approx. 0.001 - 100 ohm cm, intrinsic FZ-wafers up to > 10.000 ohm cm. Typical resistivity ranges of a wafer lot cover a (half) order of magnitude (e. g. 1 - 5 or 1 - 10 ohm cm), more narrow specs on request.
Surface: Single- and double-side polished, unpolished
Quality: “Prime”, “Test” and “Dummy”. Dummy-wafers are wafers which don’t match one or more specs required by “Prime”- or “Test”-wafers, concerning e. g. the resistivity range, thickness variation TTV, or surface quality, but are sometimes a reasonable and very cheap alternative for tests.

Services

Oxidation: 30 nm - 3 µm; dry (up to 200 nm) or dry/wet/dry (thicker SiO₂)
Silicon Nitride
Metallization: Material and thickness on request
Silicon Epitaxy
Wafer cutting: On request

Sales Units and Lead Time

We supply our wafers in units of 25 wafers (= one carrier) or single wafers in single-wafer boxes. Dummy-wafers are shipped in units of 25 or 50 wafers. For wafers with special specifications, a minimum order quantity of 25, 50 or 100 wafers is possible. A frequently revised list of stock wafers which can be shipped in few working days can be found here:

www.microchemicals.com/products/si_wafers/our_wafer_stock_list.html

For wafers we produce according your requirements, the typical lead time is 3 - 4 weeks.
Quartz- and Fused Silica Wafers

Production of Quartz Wafers
Quartz monocrystals are formed via hydrothermal synthesis. Inside the vessel (image right) filled with NaOH, quartz feed material is placed in the bottom, usually high quality broken pieces of quartz. Hereby, quartz crystallizes at a temperature of approx. 400°C and a pressure of 1000 - 1500 bar from a saturated NaOH solution at quartz seed crystals which have a slightly lower temperature than the crushed source quartz at the bottom of the container.
Quartz growth usually takes hours or days and forms monocrystals up to several kg weight. The quartz monocrystals formed hereby are cut into wafers and finally polished.

Specifications of Quartz Wafers
Crystal Orientation
Quartz is a monocrystalline material with various different crystal directions which define the orientation of the wafer surface.
Typical cuts are „X-Cut“, „Y-Cut“, „AT-Cut“, and „ST-Cut“.
Diameter
Available wafer diameters are 2, 3 and 4 inch. Other diameters or dimensions on request.
Surface
Usually, quartz wafers are double-side polished. Single-side polishing on request.

Production and Properties of Fused Silica Wafers
“Fused Silica” or “Fused Quartz” is the amorphous phase of quartz (SiO₂). In contrast to e. g. borosilicate glass, fused silica has no additives, thus is pure SiO₂.
Compared to normal glass, fused silica has a higher transmission in the ultraviolet and infrared spectrum, a very low thermal expansion coefficient, a high thermal resistance and softenig point, a superior chemical resistance and high dielectric strength.
One method for fused silica production is melting and re-solidifying of ultrapure SiO₂.
Synthetic fused silica is made from
silicon-rich chemical precursors such as SiCl₄ which are gasified and subsequently oxidized in a H₂ + O₂ atmosphere (schema previous page).

The SiO₂ dust formed hereby is fused to silica on a substrate. This technique results in an improved optical transmission in the deep ultraviolet.

The fused silica blocks are cut into wafers, and the wafers finally polished.

A frequently revised list of stock wafers which can be shipped in few working days can be found here:

www.microchemicals.com/products/si_wafers/our_wafer_stock_list.html

**Specifications of Fused Silica Wafers**

**JGS1 (Ultraviolet Grade Fused Silica)**

These wafers show a high transparency in the ultraviolet spectral range. The transmission in the VIS and UV (down to approx. 215 nm) is approx. 90 % (only reflection losses) and drops between 215 and 150 nm down to 0 %.

In the infrared range, the comparable high OH-concentration of typically 1000 ppm causes absorption bands for wavelengths > 1.2 µm.

**JGS2 (Optical Grade Fused Quartz)**

As compared with JGS1 wafers, the transmission range of significantly cheaper JGS2 wafers is shifted towards longer wavelengths: UV-absorption already starts below approx. 270 nm wavelength, while in the VIS and IR the transmission is approx. 90 % up to approx. 2 µm wavelength due to the lower OH-concentration (typ. < 300 ppm).

**JGS3 (Full Spectrum Fused Silica)**

These comparable expensive wafers with a very low OH-content (typ. < 10 ppm) show a high transparency of > 80 % over a broad spectral range of approx. 200 nm - 3 µm, and approx. 90 % in the wavelength range 250 - 2.5 µm.

**Diameter and Dimensions**

Available diameters are 2, 3, 4 and 6 inch. Other diameters as well as rectangular wafer pieces on request.

**Wafer Thicknesses**

Standard thicknesses of fused silica wafers are 500, 700 and 1000 µm. Other thicknesses on request.

**Surface**

One- or double-side polished.

A frequently revised list of stock wafers which can be shipped in few working days can be found here:

www.microchemicals.com/products/si_wafers/our_wafer_stock_list.html
Production
Float glasses are glass sheets made by floating molten glass on a bed of molten tin. Hereby the molten glass forms a floating both-side smooth ribbon with a homogeneous thickness. On its way on the tin bath, the temperature is gradually reduced from 1100 down to 600°C until the sheet can be lifted onto rollers.
After further cooling down the glass gradually to room temperature, so that it anneals without strain, the sheets are cut into the desired dimensions.

Available Specifications
Diameter and Dimensions
Available diameters are 2, 3, 4, 5, 6 and 8 inch. Other diameters as well as rectangular wafer pieces on request. Please also have a look at our stock list (www.microchemicals.com/products/si_wafers)

Wafer Thicknesses
Standard thicknesses of fused silica wafers are 500, 700 and 1100 µm. Other thicknesses on request.

Surface
One- or double-side polished.
A frequently revised list of stock wafers which can be shipped in few working days can be found here:
www.microchemicals.com/products/si_wafers/our_wafer_stock_list.html

Material Properties of Quartz, Fused Silica and Borosilicate Glass

<table>
<thead>
<tr>
<th></th>
<th>Quartz</th>
<th>Fused Silica</th>
<th>Borosilicate glass</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Composition</strong></td>
<td>100 % SiO₂</td>
<td>100 % SiO₂</td>
<td>&gt; 80 % SiO₂ &gt; 10 % B₂O₃</td>
</tr>
<tr>
<td><strong>Density (g/cm³)</strong></td>
<td>2.65</td>
<td>2.2</td>
<td>2.2</td>
</tr>
<tr>
<td><strong>Mohs hardness</strong></td>
<td>7</td>
<td>5.3 - 6.5</td>
<td>6.5</td>
</tr>
<tr>
<td><strong>Melting point (quartz). max. working temperature (glass) (°C)</strong></td>
<td>1713*</td>
<td>1400</td>
<td>400 - 500</td>
</tr>
<tr>
<td><strong>Refractive index (@ 500 - 600 nm)</strong></td>
<td>1.54</td>
<td>1.46</td>
<td>1.47</td>
</tr>
<tr>
<td><strong>Optical transmission range (µm)</strong></td>
<td>0.15 - 4</td>
<td>0.17 - 3</td>
<td>0.35 - 2</td>
</tr>
<tr>
<td><strong>Thermal expansion coefficient (10⁻⁶/K)</strong></td>
<td>8 - 13</td>
<td>0.54</td>
<td>3</td>
</tr>
<tr>
<td><strong>Heat conductivity (W/mK)</strong></td>
<td>6 - 12</td>
<td>1.38</td>
<td>1.2</td>
</tr>
<tr>
<td><strong>Dielectric strength (kV/mm)</strong></td>
<td>&gt; 1000</td>
<td>40</td>
<td>30 (@ 1 mm)</td>
</tr>
</tbody>
</table>
Disclaimer of Warranty

All information, process guides, recipes etc. given in this brochure have been added to the best of our knowledge. However, we cannot issue any guarantee concerning the accuracy of the information.

We assume no liability for any injuries/damage to staff and equipment which might stem from the information given in this brochure.

Generally speaking, it is in the responsibility of every staff member to inform herself/himself about the processes to be performed in the appropriate (technical) literature, in order to minimize any risk to man or machine.
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