SILICON INGOT PRODUCTION PROCESS FOR WAFERS

The element silicon has been the leading semiconductor material for microelectronic circuits for decades. It can be produced in an extremely pure mono-crystalline form and doped with foreign materials in a targeted manner allowing for the modulation of the electrical conductivity over approx. six orders of magnitude. A great advantage of silicon compared to other semiconductor materials such as germanium or gallium arsenide is the possibility of generating a chemically stable electrical insulator with high breakdown field strength from the substrate itself using selective thermal oxidation to SiO_2. As a substrate for microelectronic circuits, silicon must be mono-crystalline in its purest form as described in this chapter.

From Quartz to High-Purity Silicon

Origin and Occurrence of Silicon

Silicon fuses in the interior of massive suns at temperatures above 10^9 K from oxygen cores and is flung into the universe at the end of the star's life during supernova explosions. Hydrogen and helium dominate the visible matter of the universe; silicon makes up less than 0.1% of the total mass (Fig. 1).

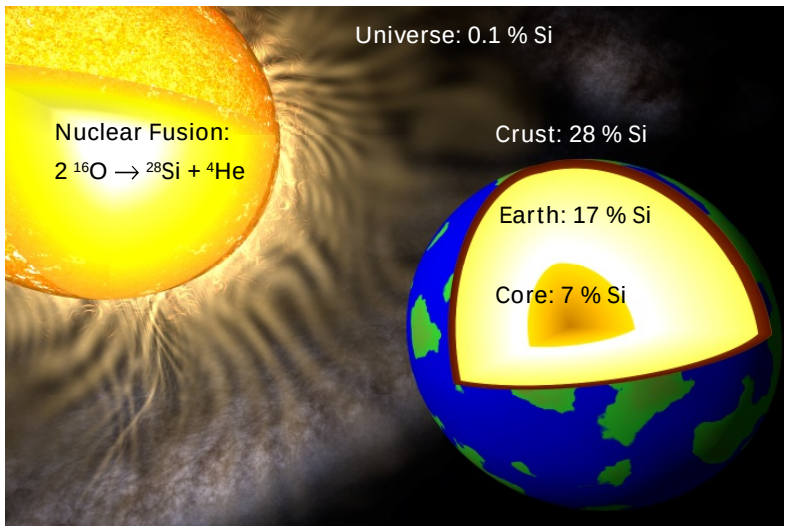


Fig. 1: The formation of silicon in the interior of massive suns and its occurrence in the entire universe and the earth

In our solar system formed from the "ashes" of earlier star explosions, silicon has been enriched, especially in the inner planets which have lost most of the volatile elements due to their proximity to the central sun. The entire planet Earth contains approx. 17 % silicon, the third most abundant element after iron and oxygen, closely followed by magnesium. In the earth's iron-based core, silicon is the second most abundant element with approx. 7 mass %.

The approximately 40 km thick earth's crust contains about 28% silicon in the form of silicate minerals or quartz (SiO_2), as well as silica ($Si(OH)_4$) as the second most common element after oxygen dissolved in the oceans. The natural occurrence of pure, i.e. elemental silicon, however, is irrelevant in terms of volume.

Production and Use of Metallurgical-Grade Silicon

For the production of elemental silicon, quartz sand (SiO_2) is reduced in smelting reduction kilns (Fig. 2) at

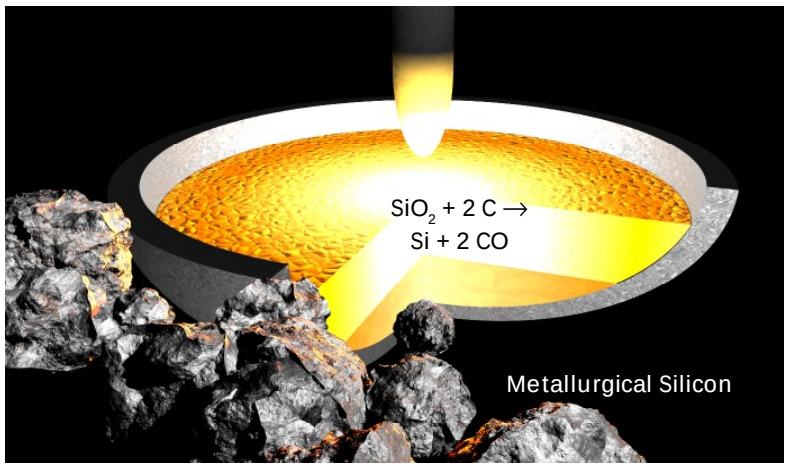


Fig. 2: Quartz sand (above) is reduced with graphite in smelting reduction furnace (schematically, right) to raw silicon.

approx. 2000°C with carbon to metallurgical-grade silicon (*metallurgical silicon*) with a purity of about 98 - 99%. With pure raw materials and electrodes, the degree of purity is also significantly higher. The majority of the world production which is done mainly in China and Russia (in 2014 about 7 million tonnes) is used as an alloy component for steel and aluminium, as well as a raw material for the production of silicones.

Only about 2% of the raw silicon is prepared for hyper-pure silicon as described in the following section, of which approximately 90% is used for the manufacture of silicon solar cells. Some 100 tonnes a year are ultimately used in the production of silicon wafers for the semiconductor sector, which this chapter is devoted to.

Preparation of Metallurgical-Grade Silicon to Hyper-pure Silicon

The concentration of impurities in the raw silicon is too high by many orders of magnitude for use as a semiconductor in the microelectronics or photovoltaics. To achieve the required electronic properties, the metallurgical-grade silicon must be “refined” to hyper-pure silicon.

In the first step to ultra-pure silicon, metallurgical-grade silicon is converted into trichlorosilane ($HSiCl_3$) via $Si + 3\ HCl \rightarrow HSiCl_3 + H_2$ at about 300°C with HCl where many impurities such as iron, which does not form volatile chlorine compounds at these temperatures, is removed. Trichlorosilane mixed with other gaseous chlorine compounds undergoes multiple distillations thereby improving the purity up to 99.9999999 % (“9N”) and is subsequently thermally decomposed to poly-crystalline silicon.

The poly-crystalline silicon formation is performed in the so-called Siemens process (Fig. 3): The purified trichlorosilane mixed in hydrogen is thermally decomposed on the surface of a heated (approx. 1100°C) *silicon rod* via $HSiCl_3 + H_2 \rightarrow Si + 3\ HCl$ to poly-crystalline silicon and HCl which corresponds to the reverse reaction of the trichlorosilane formation.

Poly-crystalline and Mono-crystalline Silicon

The poly-crystalline silicon attained in the Siemens process has, compared with electronic-grade material (purity concentration < 10^{14} cm^{-3}), a high degree of purity but crystalline grain boundaries which form electronic defects reducing the efficiency of solar cells produced with it and excluding its use in the field of microelectronics.

As the basic raw material for the production of silicon wafers as substrates for microelectronic components, only mono-crystalline silicon which is produced from poly-crystalline silicon using the Czochralski or Float-zone methods as described in the following sections comes into question.

In this case, specific and well-defined doping of the silicon with foreign atoms is also done in order to define the electrical conductivity of the wafers produced with it and to adjust it homogeneously over the entire crystal.

Fig. 3: The deposition of poly-crystalline silicon from the gaseous phase of highly purified trichlorosilane and hydrogen in the so-called Siemens process

Crystal Growth Using the Czochralski Method

Principle of the Czochralski Method

In the Czochralski method as schematically illustrated in Fig. 4, a cylindrical silicon monocrystal is pulled from a silicon melt.

First, poly-crystalline silicon (e.g. from the Siemens-process) optionally together with dopants are melted in a quartz crucible at a temperature > 1400°C in an inert

gas atmosphere (e.g. argon). The quartz crucible sits inside a graphite crucible which – due to its high heat conductivity – homogeneously transfers the heat from the surrounding heater to the quartz crucible.

The silicon melt temperature is kept constant roughly above the silicon melting point. A mono-crystalline silicon seed crystal with the desired crystal orientation (e.g. <100>, <110> or <111> as defined in section 1.4) is dipped into the melt and acts as a starting point for the crystal formation supported by the heat transfer from the melt to the already grown crystal.

The seed crystal is slowly (few cm/hour) pulled out of the melt, where the pull speed determines the crystal diameter. During crystal growth, the crystal as well as the crucible counter-rotate in order to improve the homogeneity of the crystal and its dopant concentration.

Before the crystal growth is finished, a continuous increase of the pull speed reduces the crystal diameter towards zero. This helps prevent thermal stress in the ingot which could happen by an abrupt lifting out of the melt and could destroy the crystal.

Advantages and Disadvantages of the Czochralski Method

The Czochralski technique allows big crystal diameters (currently: 18 inch = 46 cm) and – compared to the Float-zone technique described in the following section – lower production cost per wafer.

One disadvantage of the Czochralski technique is impurities such as oxygen (typ. 10^{18} cm^{-3}), carbon (typ. 10^{17} cm^{-3}) from the quartz and graphite crucible which lower the minority carrier diffusion length in the finished silicon wafer.

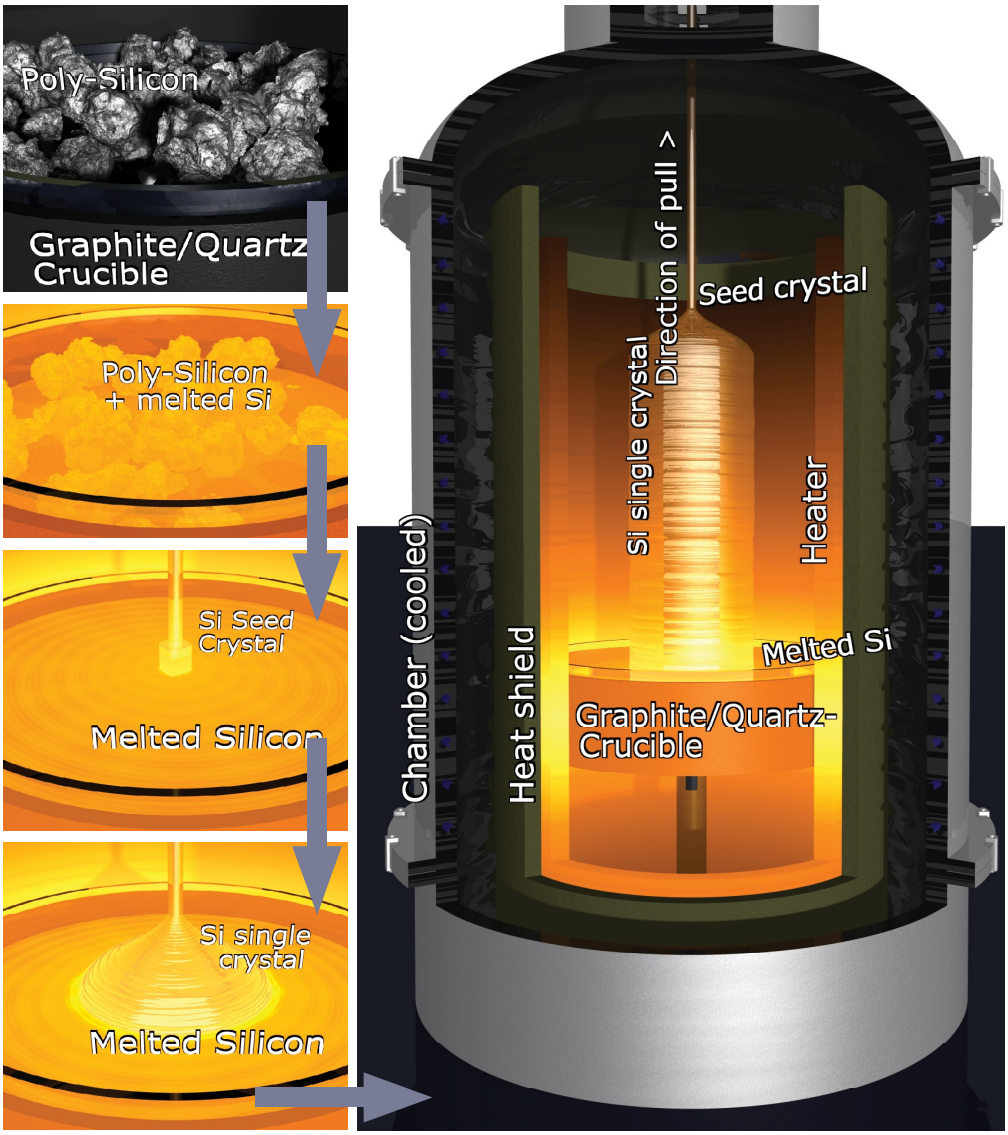


Fig. 4: A diagram of the Czochralski technique:

Top left: A quartz crucible filled with poly-crystalline silicon fragments from the Siemens process

Left 2nd from above: The silicon fragments are melted together with doping material

Left 3rd from above: A mono-crystalline seed crystal is dipped into the molten silicon

Bottom left: The seed crystal pulls a doped single crystal from the melt

Large image on the left: The schematic structure of a chamber for the crystal growing process in the Czochralski technique

Another disadvantage is a comparably low homogeneity of the axial and radial dopant concentration in the crystal caused by oscillations in the melt during crystal growth. This makes it difficult to attain high-ohmic CZ wafers with a resistivity exceeding > 100 Ohm cm. A magnetic field ("Magnetic Czochralski", MCZ) can retard these oscillations and improve the dopant homogeneity in the ingot.

Crystal Growth with the Float-zone Method

Principle of the Float-zone Method

A mono-crystalline silicon seed crystal is brought into contact with one end of a poly-crystalline silicon ingot in the float-zone (FZ) or zone melting process as schematically shown in Fig. 5. Starting from here, an RF coil melts a small region of the polysilicon which, after cooling down, forms mono-crystalline silicon with the crystallographic orientation of the seed crystal (e.g. <100>, <110> or <111> as defined in section 1.4).

The Radio-frequency (RF) coil and the melted zone move along the entire ingot. Since most impurities are less soluble in the crystal than in the melted silicon, the molten zone carries the impurities away with it. The impurities concentrate near the end of the crystal where finally they can simply be cut away. This procedure can be repeated one or more times in order to further reduce the remaining impurity concentration.

Doping is realised during crystal growth by adding dopant gases such as phosphine (PH_3), arsine (AsH_3) or diborane (B_2H_6).

Advantages and Disadvantages of the Float-zone Technique

The main advantage of the float-zone technique is the very low impurity concentration in the silicon crystal. In particular the oxygen and carbon concentration are much lower as compared to CZ silicon, since the melt does not come into contact with a quartz crucible, and no hot graphite container is used.

Additionally, the dopant concentration in the final crystal is rather homogeneous and manageable which allows very high-ohmic (1 - 10 KOhm cm) wafers as well as wafers with a narrow specified electrical resistivity.

A disadvantage of the FZ method are the relatively high cost compared with the Czochralski technique which is typically three to four times with respect to the finished wafer. For technical reasons, the diameter of the monocrystal is limited and allows for FZ wafers measuring a maximum of eight inches with the current state of technology.

Fig. 5: In zone melting techniques (*Float zone*), an induction coil melts a poly-crystalline silicon crystal longitudinally, which subsequently solidifies in a mono-crystalline manner.

Our Photoresists: Application Areas and Compatibilities

Recommended Applications [1]		Resist Family	Photoresists	Resist Film Thickness [2]	Recommended Developers [3]	Recommended Removers [4]
Positive	Improved adhesion for wet etching, no focus on steep resist sidewalls	AZ® 1500	AZ® 1505 AZ® 1512 HS AZ® 1514 H AZ® 1518	≈ 0.5 µm ≈ 1.0 - 1.5 µm ≈ 1.2 - 2.0 µm ≈ 1.5 - 2.5 µm	AZ® 351B, AZ® 326 MIF, AZ® 726 MIF, AZ® Developer	AZ® 100 Remover, TechniStrip® P1316 TechniStrip® P1331
		AZ® 4500	AZ® 4533 AZ® 4562	≈ 3 - 5 µm ≈ 5 - 10 µm	AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	
		AZ® P4000	AZ® P4110 AZ® P4330 AZ® P4620 AZ® P4903	≈ 1 - 2 µm ≈ 3 - 5 µm ≈ 6 - 20 µm ≈ 10 - 30 µm	AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	
		AZ® PL 177	AZ® PL 177	≈ 3 - 8 µm	AZ® 351B, AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	
	Spray coating	AZ® 4999		≈ 1 - 15 µm	AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	
	Dip coating	MC Dip Coating Resist		≈ 2 - 15 µm	AZ® 351B, AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	
	Steep resist sidewalls, high resolution and aspect ratio for e. g. dry etching or plating	AZ® ECI 3000	AZ® ECI 3007 AZ® ECI 3012 AZ® ECI 3027	≈ 0.7 µm ≈ 1.0 - 1.5 µm ≈ 2 - 4 µm	AZ® 351B, AZ® 326 MIF, AZ® 726 MIF, AZ® Developer	
		AZ® 9200	AZ® 9245 AZ® 9260	≈ 3 - 6 µm ≈ 5 - 20 µm	AZ® 400K, AZ® 326 MIF, AZ® 726 MIF	
	Elevated thermal softening point and high resolution for e. g. dry etching	AZ® 701 MiR	AZ® 701 MiR (14 cPs) AZ® 701 MiR (29 cPs)	≈ 0.8 µm ≈ 2 - 3 µm	AZ® 351B, AZ® 326 MIF, AZ® 726 MIF, AZ® Developer	
Positive (chem. amplified)	Steep resist sidewalls, high resolution and aspect ratio for e. g. dry etching or plating	AZ® XT	AZ® 12 XT-20PL-05 AZ® 12 XT-20PL-10 AZ® 12 XT-20PL-20 AZ® 40 XT	≈ 3 - 5 µm ≈ 6 - 10 µm ≈ 10 - 30 µm ≈ 15 - 50 µm	AZ® 400K, AZ® 326 MIF, AZ® 726 MIF	AZ® 100 Remover, TechniStrip® P1316 TechniStrip® P1331
		AZ® IPS 6050		≈ 20 - 100 µm		
Image Reversal	Elevated thermal softening point and undercut for lift-off applications	AZ® 5200	AZ® 5209 AZ® 5214	≈ 1 µm ≈ 1 - 2 µm	AZ® 351B, AZ® 326 MIF, AZ® 726 MIF	TechniStrip® Micro D2 TechniStrip® P1316 TechniStrip® P1331
		TI	TI 35ESX TI xLift-X	≈ 3 - 4 µm ≈ 4 - 8 µm		
Negative (Cross-linking)	Negative resist sidewalls in combination with no thermal softening for lift-off application	AZ® nLOF 2000	AZ® nLOF 2020 AZ® nLOF 2035 AZ® nLOF 2070	≈ 1.5 - 3 µm ≈ 3 - 5 µm ≈ 6 - 15 µm	AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	TechniStrip® NI555 TechniStrip® NF52 TechniStrip® MLO 07
		AZ® nLOF 5500	AZ® nLOF 5510	≈ 0.7 - 1.5 µm		
	Improved adhesion, steep resist sidewalls and high aspect ratios for e. g. dry etching or plating	AZ® nXT	AZ® 15 nXT (115 cPs) AZ® 15 nXT (450 cPs)	≈ 2 - 3 µm ≈ 5 - 20 µm	AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	
			AZ® 125 nXT	≈ 20 - 100 µm	AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	TechniStrip® P1316 TechniStrip® P1331 TechniStrip® NF52 TechniStrip® MLO 07

[1] In general, almost all resists can be used for almost any application. However, the special properties of each resist family makes them specially suited for certain fields of application.

[2] Resist film thickness achievable and processable with standard equipment under standard conditions. Some resists can be diluted for lower film thicknesses; with additional effort also thicker resist films can be achieved and processed.

[3] Metal Ion free (MIF) developers are significantly more expensive, and reasonable if metal ion free development is required.

Our Developers: Application Areas and Compatibilities

Inorganic Developers

(typical demand under standard conditions approx. 20 L developer per L photoresist)

AZ® Developer is based on sodium phosphate and –metasilicate, is optimized for minimal aluminum attack and is typically used diluted 1 : 1 in DI water for high contrast or undiluted for high development rates. The dark erosion of this developer is slightly higher compared to other developers.

AZ® 351B is based on buffered NaOH and typically used diluted 1 : 4 with water, for thick resists up to 1 : 3 if a lower contrast can be tolerated.

AZ® 400K is based on buffered KOH and typically used diluted 1 : 4 with water, for thick resists up to 1 : 3 if a lower contrast can be tolerated.

AZ® 303 specifically for the AZ® 111 XFS photoresist based on KOH / NaOH is typically diluted 1 : 3 - 1 : 7 with water, depending on whether a high development rate, or a high contrast is required

Metal Ion Free (TMAH-based) Developers

(typical demand under standard conditions approx. 5 - 10 L developer concentrate per L photoresist)

AZ® 326 MIF is 2.38 % TMAH- (TetraMethylAmmoniumHydroxide) in water.

AZ® 726 MIF is 2.38 % TMAH- (TetraMethylAmmoniumHydroxide) in water, with additional surfactants for rapid and uniform wetting of the substrate (e. g. for puddle development)

AZ® 826 MIF is 2.38 % TMAH- (TetraMethylAmmoniumHydroxide) in water, with additional surfactants for rapid and uniform wetting of the substrate (e. g. for puddle development) and other additives for the removal of poorly soluble resist components (residues with specific resist families), however at the expense of a slightly higher dark erosion.

Our Removers: Application Areas and Compatibilities

AZ® 100 Remover is an amine solvent mixture and standard remover for AZ® and TI photoresists. To improve its performance, AZ® 100 remover can be heated to 60 - 80°C. Because the AZ® 100 Remover reacts highly alkaline with water, it is suitable for this with respect to sensitive substrate materials such as Cu, Al or ITO only if contamination with water can be ruled out..

TechniStrip® P1316 is a remover with very strong stripping power for Novolak-based resists (including all AZ® positive resists), epoxy-based coatings, polyimides and dry films. At typical application temperatures around 75°C, TechniStrip® P1316 may dissolve cross-linked resists without residue also, e.g. through dry etching or ion implantation. TechniStrip® P1316 can also be used in spraying processes. For alkaline sensitive materials, TechniStrip® P1331 would be an alternative to the P1316. Nicht kompatibel mit Au oder GaAs.

TechniStrip® P1331 can be an alternative for TechniStrip® P1316 in case of alkaline sensitive materials. TechniStrip® P1331 is not compatible with Au or GaAs.

TechniStrip® NI555 is a stripper with very strong dissolving power for Novolak-based negative resists such as the AZ® 15 nXT and AZ® nLOF 2000 series and very thick positive resists such as the AZ® 40 XT. TechniStrip® NI555 was developed not only to peel cross-linked resists, but also to dissolve them without residues. This prevents contamination of the basin and filter by resist particles and skins, as can occur with standard strippers. TechniStrip® NI555 is not compatible with GaAs.

TechniClean™ CA25 is a semi-aqueous proprietary blend formulated to address post etch residue (PER) removal for all interconnect and technology nodes. Extremely efficient at quickly and selectively removing organo-metal oxides from Al, Cu, Ti, TiN, W and Ni.

TechniStrip™ NF52 is a highly effective remover for negative resists (liquid resists as well as dry films). The intrinsic nature of the additives and solvent make the blend totally compatible with metals used throughout the BEOL interconnects to WLP bumping applications.

TechniStrip™ Micro D2 is a versatile stripper dedicated to address resin lift-off and dissolution on negative and positive tone resist. The organic mixture blend has the particularity to offer high metal and material compatibility allowing to be used on all stacks and particularly on fragile III/V substrates for instance.

TechniStrip™ MLO 07 is a highly efficient positive and negative tone photoresist remover used for IR, III/V, MEMS, Photonic, TSV mask, solder bumping and hard disk stripping applications. Developed to address high dissolution performance and high material compatibility on Cu, Al, Sn/Ag, Alumina and common organic substrates.

Our Wafers and their Specifications

Silicon-, Quartz-, Fused Silica and Glass Wafers

Silicon wafers are either produced via the Czochralski- (CZ-) or Float zone- (FZ-) method. The more expensive FZ wafers are primarily reasonable if very high-ohmic wafers (> 100 Ohm cm) are required.

Quartz wafers are made of monocrystalline SiO_2, main criterion is the crystal orientation (e. g. X-, Y-, Z-, AT- or ST-cut)

Fused silica wafers consist of amorphous SiO_2. The so-called JGS2 wafers have a high transmission in the range of ≈ 280 - 2000 nm wavelength, the more expensive JGS1 wafers at ≈ 220 - 1100 nm.

Our glass wafers, if not otherwise specified, are made of borosilicate glass.

Specifications

Common parameters for all wafers are diameter, thickness and surface (1- or 2-side polished). Fused silica wafers are made either of JGS1 or JGS2 material, for quartz wafers the crystal orientation needs to be defined. For silicon wafers, beside the crystal orientation (<100> or <111>) the doping (n- or p-type) as well as the resistivity (Ohm cm) are selection criteria.

Prime- ,Test-, and Dummy Wafers

Silicon wafers usually come as „Prime-grade“ or „Test-grade“, latter mainly have a slightly broader particle specification. „Dummy-Wafers“ neither fulfill Prime- nor Test-grade for different possible reasons (e. g. very broad or missing specification of one or several parameters, reclaim wafers, no particle specification) but might be a cheap alternative for e. g. resist coating tests or equipment start-up.

Our Silicon-, Quartz-, Fused Silica and Glass Wafers

Our frequently updated wafer stock list can be found here: **è** www.microchemicals.com/products/wafers/waferlist.html

Further Products from our Portfolio

Plating

Plating solutions for e. g. gold, copper, nickel, tin or palladium: **è** www.microchemicals.com/products/electroplating.html

Solvents (MOS, VLSI, ULSI)

Acetone, isopropyl alcohol, MEK, DMSO, cyclopentanone, butylacetate, ... **è** www.microchemicals.com/products/solvents.html

Acids and Bases (MOS, VLSI, ULSI)

Hydrochloric acid, sulphuric acid, nitric acid, KOH, TMAH, … **è** www.microchemicals.com/products/etchants.html

Etching Mixtures

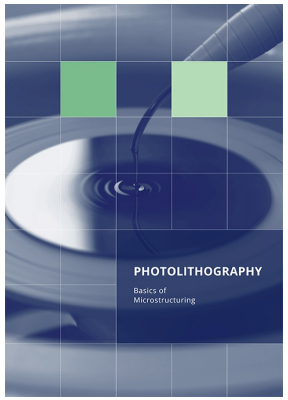
for e. g. chromium, gold, silicon, copper, titanium, ... **è** www.microchemicals.com/products/etching_mixtures.html

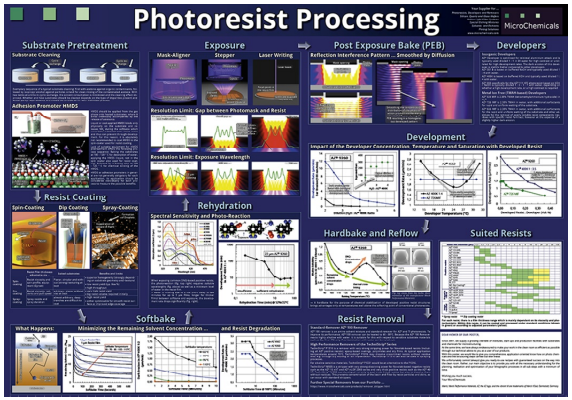
Further Information

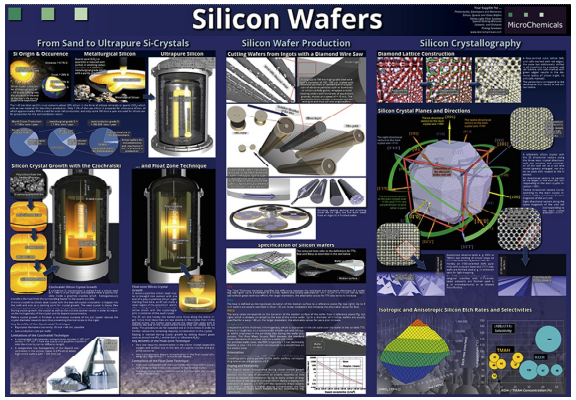
Technical Data Sheets: www.microchemicals.com/downloads/product_data_sheets/photoresists.html

Material Safety Data Sheets (MSDS): www.microchemicals.com/downloads/safety_data_sheets/msds_links.html

Our Photolithography Book and -Posters







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