SILICON WAFER PRODUCTION AND SPECIFICATIONS

Silicon Wafer Production

From Ingot to Cylinder

The monocrystals grown with the Czochralski or Float-zone technique are ground to the desired diameter and cut into shorter workable cylinders with e.g. a band saw and ground to a certain diameter.

Flats

An orientation flat is added to indicate the crystal orientation (Fig. 16), while wafers with an 8 inch diameter and above use a single notch to convey wafer orientation, independent from the doping type.

Two common techniques are applied for wafer dicing: Inside hole saw and wire saw, both explained in the following sections.

Inside Hole Saw (Annular Saw)

The wafers are sawed inside a circular blade whose cutting edge is filled with diamond splinters (Fig. 17).

After sawing, the wafer surfaces are already relatively flat and smooth, so the subsequent lapping of the surfaces takes less time and effort.

However, only one wafer per annular saw can be cut at the same time, so this technique has a comparably low throughput which makes the wafers more expensive compared to wafers cut by a wire saw.

Wire Saw

In order to increase throughput, wire saws with many parallel wires are used which cut many wafers at once (Fig. 18). A long (up to 100 km) high-grade steel wire with a diameter of 100 - 200 μm is wrapped around rotating rollers with hundreds of equidistant grooves at a speed of typically 10 m/s. The mounted silicon cylinder is drained into the wire grid and thus cut into single wafers.
The wire is either coated with diamond splinters or wetted with a suspension of abrasive particles such as diamonds or silicon carbide grains, and a carrier (glycol or oil). The main advantage of this sawing method is that hundreds of wafers can be cut at a time with one wire. However, the attained wafer surface is less smooth and more bumpy as compared to wafers cut by an annular saw, so the subsequent wafer lapping takes more time.

**Lapping**

After dicing, the wafers are lapped on both sides in order to i) remove the surface silicon which has been cracked or otherwise damaged by the slicing process (e.g. grooves by the wire saw) and ii) thinned to the desired wafer thickness.

Several wafers at a time are lapped in between two counter-rotating pads by a slurry consisting of e.g. Al₂O₃ or SiC abrasive grains with a defined size distribution.

**Etching**

Wafer dicing and lapping degrade the silicon surface crystal structure, so subsequently the wafers are...
etched in either KOH- or HNO$_3$/HF based etchants in order to remove the damaged surface.

**Polishing**
After etching, both wafer surfaces appear like the rear side of finished single-side polished wafer. In order to attain the super-flat, mirrored surface with a remaining roughness on atomic scale, the wafers have to be polished. Wafer polishing is a multi-step process using an ultra-fine slurry with 10 - 100 nm sized grains consisting of e.g. Al$_2$O$_3$, SiO$_2$ or CeO$_2$ which, combined with pressure, erode and mechanically and chemically smoothen the wafer surface between two rotating pads.

**Cleaning**
Finally, the wafers are cleaned with ultra-pure chemicals in order to remove the polishing agents thereby making them residual-free and guaranteeing the particle specification.

**Silicon Wafer Specifications**

**Diameter**
The diameter of the silicon wafers are specified either in inches or mm. Although an inch is 25.4 mm, the diameters of wafers in inches are usually multiples of 25.0 mm (e.g. 4 inches = 100 mm), which should be clarified beforehand with the supplier.
The tolerance of the diameter is typically +/- 0.5 mm.

**Orientation**
The wafer orientation (e.g. $<$100>, $<$110>$ or $<$111>$) denotes the crystallographic plane parallel to the wafer surface. For certain applications, a defined tilting to the main crystallographic plane may be desirable, but usually an attempt is made to orient the wafer surface as precisely as possible to the main crystal plane; corresponding tolerances are generally +/- 0.5°.

**Surfaces**
Usually both sides of silicon wafers are at least lapped and etched. Surface polishing is performed either on one (SSP = Single-Side Polished) or both sides, DSP = Double-Side Polished). The roughness of the polished side(s) is approximately 1 nm (0.5 nm is technically feasible), of the unpolished side in the range of several µm.

**Doping and Resistivity**
The dopant atoms incorporated during silicon crystal growth increase the electrical conductivity via an increase in the free electron (in the case of phosphor or arsenic dopants) or hole (boron as dopant) concen-
Concentration by up to many orders of magnitude beyond the value of undoped silicon. Below a doping concentration of approx. \( c = 10^{16} \text{ cm}^{-3} \) the resistivity drops reciprocally with \( c \), towards a higher doping concentration the free carrier mobility drops which flattens the \( R(c) \) dependency (Fig. 21). Since the doping concentration is not perfectly homogeneous but axially and radially varies in the silicon crystal, the wafers are specified to a certain range (for CZ wafers typically within one order of magnitude, such as 1 - 10 ohm cm), through defined manufacturing processes and, where appropriate, a subsequent sorting of the wafers of a batch can even span a factor of approximately two.

**Thickness**

The usual thickness of Si wafers is dependent on their diameter due to reasons of mechanical stability during production and further processing, and is about 280 \( \mu \text{m} \) (for wafers with 2 inch diameter), 380 \( \mu \text{m} \) (3 inch), 525 \( \mu \text{m} \) (4 inch), 675 \( \mu \text{m} \) (6 inch) and 725 \( \mu \text{m} \) (8 inch).

Within the context of conventional production methods, the wafer thickness is limited upwards to approx. 2 mm, since the polishing machines cannot accommodate thicker wafers. A limitation of the wafer thickness downwards to approx. 200 \( \mu \text{m} \) as given by many manufacturers, is due to the risk of fracture.
during grinding and polishing.

The thickness tolerance corresponds to the variation of the thickness measured in the wafer centre of a batch. Usually this parameter is specified with +/-25 µm independent of the wafer diameter, the measured values are often at approx. +/-15 µm.

This distribution does not, however, tell us how much a wafer deviates from the ideal cylindrical shape. With the assistance of the planes and surfaces defined in Fig. 20, this identifies the values TTV, bow and warp described in the following.

**TTV**

Die Total Thickness Variation specifies the difference \( d_1 - d_2 \) (Fig. 22 top) between the minimum and maximum thickness of a wafer.

Up to a diameter of 4 inches, wafers are usually specified on TTV <10 µm (TTV <5 µm can be realised without great technical effort). For larger diameters, the attainable values for TTV also increase.

**Bow**

The bow is defined by \( d_3 + d_4 \) (Fig. 22 centre) as the maximum deviation of the median surface to a reference plane.

Up to a diameter of 4 inch wafers are usually specified on Bow < 40 microns, with larger diameters also increase the recoverable values for Bow.

**Warp**

The value \( d_5 + d_6 \) (Fig. 22 below) corresponds to the deviation of the median surface of the wafer from a reference plane which is already corrected by the bow of the entire wafer.

Up to a diameter of 4 inches, wafers are usually specified for a warp < 40 µm. For larger diameters, the attainable values for warp also increase.

**Micro-roughness**

Irrespective of the thickness inhomogeneity which is expressed in the cm scale over the wafer in the variable TTV, there is a roughness on a substantially smaller µm and nm scale, which originates in the polishing step during the wafer production.

The (Root Mean Square, RMS) denotes the standard height deviation of a surface scan on a wafer.

For polished wafer sides, the RMS is typically specified at <1 nm; technically feasible is also <0.5 nm which corresponds to a smoothness on the atomic scale.
Our Photoresists: Application Areas and Compatibilities

<table>
<thead>
<tr>
<th>Recommended Applications^1</th>
<th>Resist Family</th>
<th>Photosists</th>
<th>Resist Film Thickness^2</th>
<th>Recommended Developers^3</th>
<th>Recommended Removers^4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Improved adhesion for wet etching, no focus on steep resist sidewalls</td>
<td>AZ® 1500</td>
<td>AZ® 1505</td>
<td>≈ 0.5 µm</td>
<td>AZ® 351B, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF</td>
<td>AZ® 100 Remover, TechniStrip® P1316, TechniStrip® P1331</td>
</tr>
<tr>
<td></td>
<td>AZ® 1512 HS</td>
<td>AZ® 1514 H</td>
<td>≈ 1.0 - 1.5 µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® 1518</td>
<td></td>
<td>≈ 1.2 - 2.0 µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® 4500</td>
<td>AZ® 4533</td>
<td>≈ 3 - 5 µm</td>
<td>AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® 4562</td>
<td></td>
<td>≈ 5 - 10 µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spraying</td>
<td>AZ® P4000</td>
<td>AZ® P4110</td>
<td>≈ 1 - 2 µm</td>
<td>AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® P4330</td>
<td>AZ® P4620</td>
<td>≈ 3 - 5 µm</td>
<td>AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® P4903</td>
<td></td>
<td>≈ 6 - 20 µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® PL 177</td>
<td>AZ® PL 177</td>
<td>≈ 6 - 20 µm</td>
<td>AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® 4999</td>
<td></td>
<td>≈ 10 - 30 µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dip coating</td>
<td>MC Dip Coating Resist</td>
<td></td>
<td>≈ 1 - 3 µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® ECI 3000</td>
<td>AZ® ECI 3007</td>
<td>≈ 0.7 µm</td>
<td>AZ® 351B, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® ECI 3012</td>
<td>AZ® ECI 3027</td>
<td>≈ 1.0 - 1.5 µm</td>
<td>AZ® 351B, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® 9200</td>
<td>AZ® 9245</td>
<td>≈ 3 - 6 µm</td>
<td>AZ® 400K, AZ® 326 MIF, AZ® 726 MIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® 9260</td>
<td></td>
<td>≈ 5 - 20 µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® 701 MIF (14 cPs)</td>
<td>AZ® 701 MIR (14 cPs)</td>
<td>≈ 0.8 µm</td>
<td>AZ® 351B, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® 701 MIF (29 cPs)</td>
<td></td>
<td>≈ 2 - 3 µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Positive (chem. amplified)</td>
<td>Steep resist sidewalls, high resolution and aspect ratio for e. g. dry etching or plating</td>
<td>AZ® XT</td>
<td>AZ® 12 XT-20PL-05</td>
<td>AZ® 400K, AZ® 326 MIF, AZ® 726 MIF</td>
<td>AZ® 100 Remover, TechniStrip® P1316, TechniStrip® P1331</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AZ® 12 XT-20PL-10</td>
<td>≈ 3 - 6 µm</td>
<td>AZ® 400K, AZ® 326 MIF, AZ® 726 MIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AZ® 12 XT-20PL-20</td>
<td>≈ 6 - 10 µm</td>
<td>AZ® 400K, AZ® 326 MIF, AZ® 726 MIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AZ® 40 XT</td>
<td>≈ 10 - 30 µm</td>
<td>AZ® 400K, AZ® 326 MIF, AZ® 726 MIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>≈ 15 - 50 µm</td>
<td>AZ® 400K, AZ® 326 MIF, AZ® 726 MIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>AZ® IPS 6050</td>
<td></td>
<td>≈ 20 - 100 µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Image Reversal</td>
<td>Elevated thermal softening point and undercut for lift-off applications</td>
<td>AZ® 5200</td>
<td>AZ® 5209</td>
<td>AZ® 351B, AZ® 326 MIF, AZ® 726 MIF</td>
<td>TechniStrip® Micro D2, TechniStrip® P1316, TechniStrip® P1331</td>
</tr>
<tr>
<td></td>
<td>TI</td>
<td>TI 35ESX</td>
<td></td>
<td>AZ® 351B, AZ® 326 MIF, AZ® 726 MIF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TI xLift-X</td>
<td></td>
<td>AZ® 351B, AZ® 326 MIF, AZ® 726 MIF</td>
<td></td>
</tr>
<tr>
<td>Negative (Crosslinking)</td>
<td>Negative resist sidewalls in combination with no thermal softening for lift-off application</td>
<td>AZ® nLOF 2000</td>
<td>AZ® nLOF 2020</td>
<td>AZ® 326 MF, AZ® 726 MF, AZ® 826 MF</td>
<td>TechniStrip® N555, TechniStrip® NF52, TechniStrip® MLO 07</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AZ® nLOF 2035</td>
<td></td>
<td>AZ® 326 MF, AZ® 726 MF, AZ® 826 MF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AZ® nLOF 2070</td>
<td></td>
<td>AZ® 326 MF, AZ® 726 MF, AZ® 826 MF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AZ® nLOF 5510</td>
<td></td>
<td>AZ® 326 MF, AZ® 726 MF, AZ® 826 MF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Improved adhesion, steep resist sidewalls and high aspect ratios for e. g. dry etching or plating</td>
<td>AZ® nXT</td>
<td>AZ® 15 nXT (115 cPs)</td>
<td>AZ® 326 MF, AZ® 726 MF, AZ® 826 MF</td>
<td>TechniStrip® P1316, TechniStrip® P1331, TechniStrip® NF52, TechniStrip® MLO 07</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AZ® 15 nXT (450 cPs)</td>
<td></td>
<td>AZ® 326 MF, AZ® 726 MF, AZ® 826 MF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AZ® 125 nXT</td>
<td></td>
<td>AZ® 326 MF, AZ® 726 MF, AZ® 826 MF</td>
<td></td>
</tr>
</tbody>
</table>

Our Developers: Application Areas and Compatibilities

Inorganic Developers

AZ® Developer is based on sodium phosphate and –metasilicate, is optimized for minimal aluminum attack and is typically used diluted 1:1 in DI water for high contrast or undiluted for high development rates. The dark erosion of this developer is slightly higher compared to other developers. AZ® 351B is based on buffered NaOH and typically used diluted 1:4 with water, for thick resists up to 1:3 if a lower contrast can be tolerated. AZ® 400K is based on buffered KOH and typically used diluted 1:4 with water, for thick resists up to 1:3 if a lower contrast can be tolerated. AZ® 303 specifically for the AZ® 111 XFS photoresist based on KOH / NaOH is typically diluted 1:3 - 1:7 with water, depending on whether a high development rate, or a high contrast is required

Metal Ion Free (TMAH-based) Developers

AZ® 326 MIF is 2.38 % TMAH- (TetramethylAmmoniumHydroxide) in water.
AZ® 726 MIF is 2.38 % TMAH- (TetraMethylAmmoniumHydroxide) in water, with additional surfactants for rapid and uniform wetting of the substrate (e.g. for puddle development).

AZ® 826 MIF is 2.38 % TMAH- (TetraMethylAmmoniumHydroxide) in water, with additional surfactants for rapid and uniform wetting of the substrate (e.g. for puddle development) and other additives for the removal of poorly soluble resist components (residues with specific resist families), however at the expense of a slightly higher dark erosion.

Our Removers: Application Areas and Compatibilities

AZ® 100 Remover is an amine solvent mixture and standard remover for AZ® and TI photoresists. To improve its performance, AZ® 100 remover can be heated to 60 - 80°C. Because the AZ® 100 Remover reacts highly alkaline with water, it is suitable for this with respect to sensitive substrate materials such as Cu, Al or ITO only if contamination with water can be ruled out.

TechniStrip® P1316 is a remover with very strong stripping power for Novolak-based resists (including all AZ® positive resists), epoxy-based coatings, polyimides and dry films. At typical application temperatures around 75°C, TechniStrip® P1316 may dissolve cross-linked resists without residue also, e.g. through dry etching or ion implantation. TechniStrip® P1316 can also be used in spraying processes. For alkaline sensitive materials, TechniStrip® P1313 would be an alternative to the P1316. Nicht kompatibel mit Au oder GaAs.

TechniStrip® P1331 can be an alternative for TechniStrip® P1316 in case of alkaline sensitive materials. TechniStrip® P1331 is not compatible with Au or GaAs.

TechniStrip® N555 is a stripper with very strong dissolving power for Novolak-based negative resists such as the AZ® 15 nXT and AZ® nLOF 2000 series and very thick positive resists such as the AZ® 40 XT. TechniStrip® N555 was developed not only to peel cross-linked resists, but also to dissolve them without residues. This prevents contamination of the basin and filter by resist particles and skins, as can occur with standard strippers. TechniStrip® N555 is not compatible with Au or GaAs.

TechniClean™ CA25 is a semi-aqueous proprietary blend formulated to address post etch residue (PER) removal for all interconnect and technology nodes. Extremely efficient at quickly and selectively removing organo-metal oxides from Al, Cu, Ti, TiN, W and Ni.

TechniStrip™ NFS2 is a highly effective remover for negative resists (liquid resists as well as dry films). The intrinsic nature of the additives and solvent make the blend totally compatible with metals used throughout the BEOL interconnects to WLP bumping applications.

TechniStrip™ Micro D2 is a versatile stripper dedicated to address resin lift-off and dissolution on negative and positive tone resist. The organic mixture blend has the particularity to offer high metal and material compatibility allowing to be used on all stacks and particularly on fragile III/V substrates for instance.

TechniStrip™ MLO 07 is a highly efficient positive and negative tone photoresist remover used for IR, III/V, MEMS, Photonic, TSV mask, solder bumping and hard disk stripping applications. Developed to address high dissolution performance and high material compatibility on Cu, Al, Sn/Ag, Alumina and common organic substrates.

Our Wafers and their Specifications

Silicon-, Quartz-, Fused Silica and Glass Wafers

Silicon wafers are either produced via the Czochralski- (CZ-) or Float zone- (FZ-) method. The more expensive FZ wafers are primarily reasonable if very high-ohmic wafers (> 100 Ohm cm) are required.

Quartz wafers are made of monocrystalline SiO\(_2\), main criterion is the crystal orientation (e. g. X-, Y-, Z-, AT- or ST-cut).

Fused silica wafers consist of amorphous SiO\(_2\). The so-called JGS2 wafers have a high transmission in the range of \(\approx 280 - 2000\) nm wavelength, the more expensive JGS1 wafers at \(\approx 220 - 1100\) nm.

Our glass wafers, if not otherwise specified, are made of borosilicate glass.

Specifications

Common parameters for all wafers are diameter, thickness and surface (1- or 2-side polished). Fused silica wafers are made either of JGS1 or JGS2 material, for quartz wafers the crystal orientation (<100> or <111>) and the doping (n- or p-type) as well as the resistivity (Ohm cm) are selection criteria.

Prime-, Test-, and Dummy Wafers

Silicon wafers usually come as „Prime-grade“ or „Test-grade“, latter mainly have a slightly broader particle specification. „Dummy-Wafers“ neither fulfill Prime- nor Test-grade for different possible reasons (e. g. very broad or missing specification of one or several parameters, reclaim wafers, no particle specification) but might be a cheap alternative for e. g. resist coating tests or equipment start-up.

Our Silicon-, Quartz-, Fused Silica and Glass Wafers

Our frequently updated wafer stock list can be found here: www.microchemicals.com/products/wafers/waferlist.html

Further Products from our Portfolio

Plating

Plating solutions for e.g. gold, copper, nickel, tin or palladium: www.microchemicals.com/products/electroplating.html

Solvents (MOS, VLSI, ULSI)

Acetone, isopropyl alcohol, MEK, DMSO, cyclopentanone, butylacetate, ... www.microchemicals.com/products/solvents.html

Acids and Bases (MOS, VLSI, ULSI)

Hydrochloric acid, sulphuric acid, nitric acid, KOH, TMAH, ... www.microchemicals.com/products/etchants.html

Etching Mixtures

for e.g. chromium, gold, silicon, copper, titanium, ... www.microchemicals.com/products/etching_mixtures.html
Further Information


Our Photolithography Book and -Posters

We see it as our main task to make you understand all aspects of microstructuring in an application-oriented way. At present, we have implemented this claim with our book Photolithography on over 200 pages, as well as attractively designed DIN A0 posters for your office or laboratory. We will gladly send both of these to you free of charge as our customer (if applicable, we charge shipping costs for non-European deliveries):

www.microchemicals.com/downloads/brochures.html
www.microchemicals.com/downloads/posters.html

Thank you for your interest!

Disclaimer of Warranty & Trademarks

All information, process descriptions, recipes, etc. contained in this book are compiled to the best of our knowledge. Nevertheless, we cannot guarantee the correctness of the information. Particularly with regard to the formulations for chemical (etching) processes we assume no guarantee for the correct specification of the components, the mixing conditions, the preparation of the batches and their application.

The safe sequence of mixing components of a recipe usually does not correspond to the order of their listing. We do not warrant the full disclosure of any indications (among other things, health, work safety) of the risks associated with the preparation and use of the recipes and processes. The information in this book is based on our current knowledge and experience. Due to the abundance of possible influences in the processing and application of our products, they do not exempt the user from their own tests and trials. A guarantee of certain properties or suitability for a specific application cannot be derived from our data. As a matter of principle, each employee is required to provide sufficient information in advance in the appropriate cases in order to prevent damage to persons and equipment. All descriptions, illustrations, data, conditions, weights, etc. can be changed without prior notice and do not constitute a contractually agreed product characteristics. The user of our products is responsible for any proprietary rights and existing laws.

Merck, Merck Performance Materials, AZ, the AZ logo, and the vibrant M are trademarks of Merck KGaA, Darmstadt, Germany

MicroChemicals GmbH
Nikolaus-Otto-Str. 39
89079, Ulm
Germany

Fon: +49 (0)731 977 343 0
Fax: +49 (0)731 977 343 29
e-Mail: info@microchemicals.net
Internet: www.microchemicals.net