

SILICON WAFER PRODUCTION AND SPECIFICATIONS

Silicon Wafer Production

From Ingot to Cylinder

The monocrystals grown with the Czochralski or Float-zone technique are ground to the desired diameter and cut into shorter workable cylinders with e.g. a band saw and ground to a certain diameter.



Fig. 15: Grinding, sawing, etching and polished (from left to right) are the work steps from an ingot to a finished wafer

Flats

An orientation flat is added to indicate the crystal orientation (Fig. 16), while wafers with an 8 inch diameter and above use a single notch to convey wafer orientation, independent from the doping type.

Two common techniques are applied for wafer dicing: Inside hole saw and wire saw, both explained in the following sections.

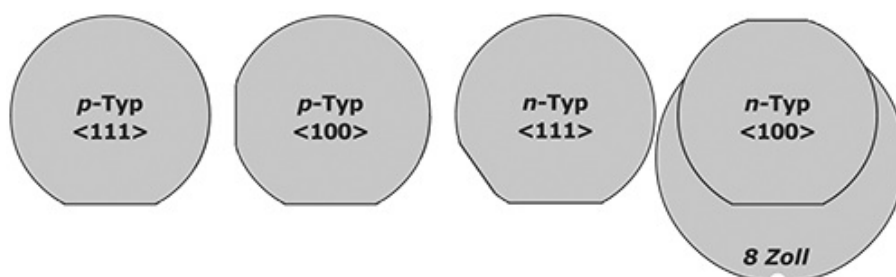


Fig. 16: The usual ("SEMI-standard") arrangement of the flats with wafers in dependency on crystal orientation and doping

Inside Hole Saw (Annular Saw)

The wafers are sawed inside a circular blade whose cutting edge is filled with diamond splinters (Fig. 17).

After sawing, the wafer surfaces are already relatively flat and smooth, so the subsequent lapping of the surfaces takes less time and effort.

However, only one wafer per annular saw can be cut at the same time, so this technique has a comparably low throughput which makes the wafers more expensive compared to wafers cut by a wire saw.

Wire Saw

In order to increase throughput, wire saws with many parallel wires are used which cut many wafers at once (Fig. 18). A long (up to 100 km) high-grade steel wire with a diameter of e 100 - 200 μm is wrapped around rotating rollers with hundreds of equidistant grooves at a speed of typically 10 m/s. The mounted silicon cylinder is drained into the wire grid and thus cut into single wafers.

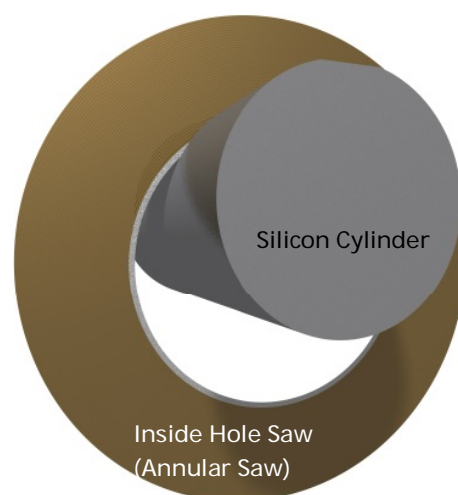


Fig. 17: Diagram of an inside hole saw with the centrally mounted silicon ingot

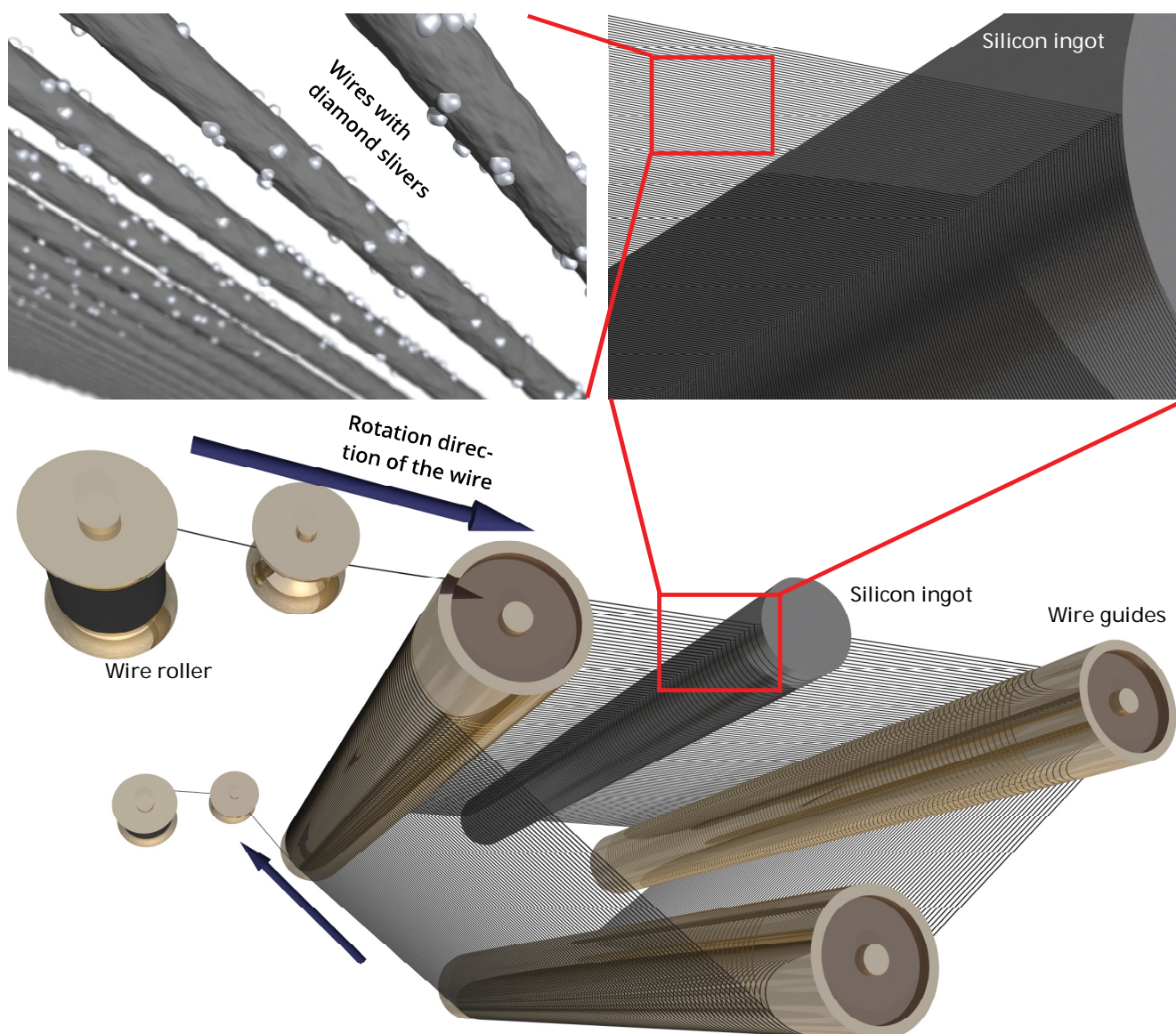


Fig. 18: Diagram of the wire saw process. The two detailed enlargements above show the proportions between the Si-cylinder, wire spacing and wire diameter approximately to scale.

The wire is either coated with diamond splinters or wetted with a suspension of abrasive particles such as diamonds or silicon carbide grains, and a carrier (glycol or oil).

The main advantage of this sawing method is that hundreds of wafers can be cut at a time with one wire. However, the attained wafer surface is less smooth and more bumpy as compared to wafers cut by an annular saw, so the subsequent wafer lapping takes more time.

Lapping

After dicing, the wafers are lapped on both sides in order to i) remove the surface silicon which has been cracked or otherwise damaged by the slicing process (e.g. grooves by the wire saw) and ii) thinned to the desired wafer thickness.

Several wafers at a time are lapped in between two counter-rotating pads by a slurry consisting of e.g. Al_2O_3 or SiC abrasive grains with a defined size distribution.

Etching

Wafer dicing and lapping degrade the silicon surface crystal structure, so subsequently the wafers are

etched in either KOH- or HNO_3/HF based etchants in order to remove the damaged surface.

Polishing

After etching, both wafer surfaces appear like the rear side of finished single-side polished wafer. In order to attain the super-flat, mirrored surface with a remaining roughness on atomic scale, the wafers have to be polished. Wafer polishing is a multi-step process using an ultra-fine slurry with 10 - 100 nm sized grains consisting of e.g. Al_2O_3 , SiO_2 or CeO_2 which, combined with pressure, erode and mechanically and chemically smoothen the wafer surface between two rotating pads.

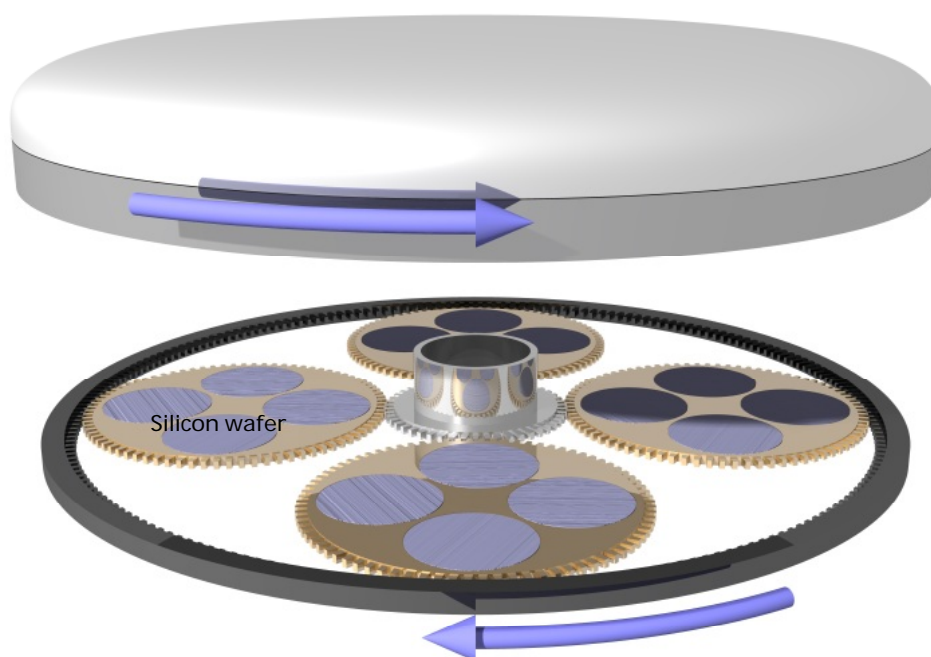


Fig. 19: Diagram of a grinder (In principle also a polishing machine) for the wafer. The opposing and superimposed rotation ensures uniform material removal from the wafer surface without preference for one particular direction.

Cleaning

Finally, the wafers are cleaned with ultra-pure chemicals in order to remove the polishing agents thereby making them residual-free and guaranteeing the particle specification.

Silicon Wafer Specifications

Diameter

The diameter of the silicon wafers are specified either in inches or mm. Although an inch is 25.4 mm, the diameters of wafers in inches are usually multiples of 25.0 mm (e.g. 4 inches = 100 mm), which should be clarified beforehand with the supplier.

The tolerance of the diameter is typically ± 0.5 mm.

Orientation

The wafer orientation (e.g. $\langle 100 \rangle$, $\langle 110 \rangle$ or $\langle 111 \rangle$) denotes the crystallographic plane parallel to the wafer surface. For certain applications, a defined tilting to the main crystallographic plane may be desirable, but usually an attempt is made to orient the wafer surface as precisely as possible to the main crystal plane; corresponding tolerances are generally $\pm 0.5^\circ$.

Surfaces

Usually both sides of silicon wafers are at least lapped and etched. Surface polishing is performed either on one (SSP = *Single-Side Polished*) or both sides, DSP = *Double-Side Polished*).

The roughness of the polished side(s) is approximately 1 nm (0.5 nm is technically feasible), of the unpolished side in the range of several μm .

Doping and Resistivity

The dopant atoms incorporated during silicon crystal growth increase the electrical conductivity via an increase in the free electron (in the case of phosphor or arsenic dopants) or hole (boron as dopant) concen-

tration by up to many orders of magnitude beyond the value of undoped silicon. Below a doping concentration of approx. $c = 10^{16} \text{ cm}^{-3}$ the resistivity drops reciprocally with c , towards a higher doping concentration the free carrier mobility drops which flattens the $R(c)$ dependency (Fig. 21). Since the doping concentration is not perfectly homogeneous but axially and radially varies in the silicon crystal, the wafers are specified to a certain range (for CZ wafers typically within one order of magnitude, such as 1 - 10 ohm cm), through defined manufacturing processes and, where appropriate, a subsequent sorting of the wafers of a batch can even span a factor of approximately two.

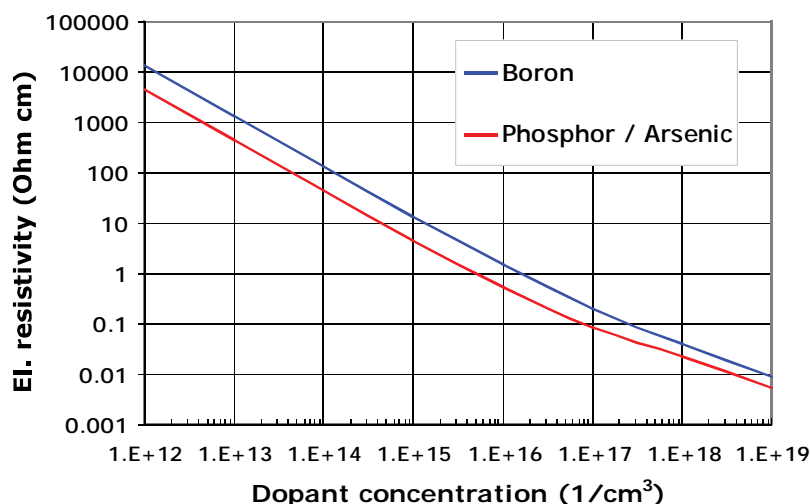


Fig. 21: The dependency of the el. resistance of the doping concentration (boron and phosphorus or arsenic) in crystalline silicon. Because at very high doping concentrations, these act as imperfections which reduce the free carrier mobility, the specific resistance shrinks more and more slowly from a doping concentration of approx. 10^{16} .

Thickness

The usual thickness of Si wafers is dependent on their diameter due to reasons of mechanical stability during production and further processing, and is about 280 μm (for wafers with 2 inch diameter), 380 μm (3 inch), 525 μm (4 inch), 675 μm (6 inch) and 725 μm (8 inch).

Within the context of conventional production methods, the wafer thickness is limited upwards to approx. 2 mm, since the polishing machines cannot accommodate thicker wafers. A limitation of the wafer thickness downwards to approx. 200 μm as given by many manufacturers, is due to the risk of fracture

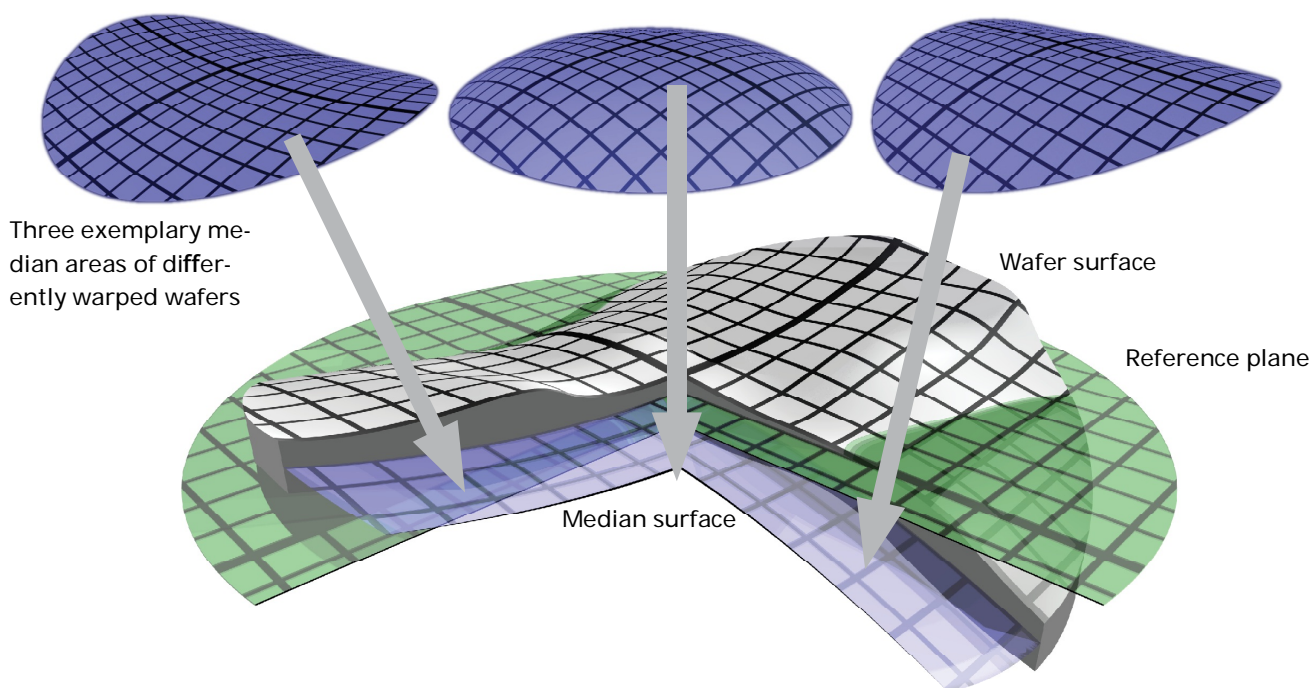


Fig. 20: In addition to the thickness inhomogeneity of a wafer (grey form), a wafer is "warped" in itself in various ways, which can be represented by so-called median surfaces (blue), which ignore the thickness inhomogeneity. The deviation of the median surface of a wafer to the planar reference surface (green) defines the parameters of bow and warp.

during grinding and polishing.

The thickness tolerance corresponds to the variation of the thickness measured in the wafer centre of a batch. Usually this parameter is specified with $\pm 25 \mu\text{m}$ independent of the wafer diameter, the measured values are often at approx. $\pm 15 \mu\text{m}$.

This distribution does not, however, tell us how much a wafer deviates from the ideal cylindrical shape. With the assistance of the planes and surfaces defined in Fig. 20, this identifies the values TTV, bow and warp described in the following.

TTV

The *Total Thickness Variation* specifies the difference $d_1 - d_2$ (Fig. 22 top) between the minimum and maximum thickness of a wafer.

Up to a diameter of 4 inches, wafers are usually specified on $\text{TTV} < 10 \mu\text{m}$ ($\text{TTV} < 5 \mu\text{m}$ can be realised without great technical effort). For larger diameters, the attainable values for TTV also increase.

Bow

The *bow* is defined by $d_3 + d_4$ (Fig. 22 centre) as the maximum deviation of the median surface to a reference plane.

Up to a diameter of 4 inch wafers are usually specified on $\text{Bow} < 40 \mu\text{m}$, with larger diameters also increase the recoverable values for Bow.

Warp

The value $d_5 + d_6$ (Fig. 22 below) corresponds to the deviation of the median surface of the wafer from a reference plane which is already corrected by the bow of the entire wafer.

Up to a diameter of 4 inches, wafers are usually specified for a warp $< 40 \mu\text{m}$. For larger diameters, the attainable values for warp also increase.

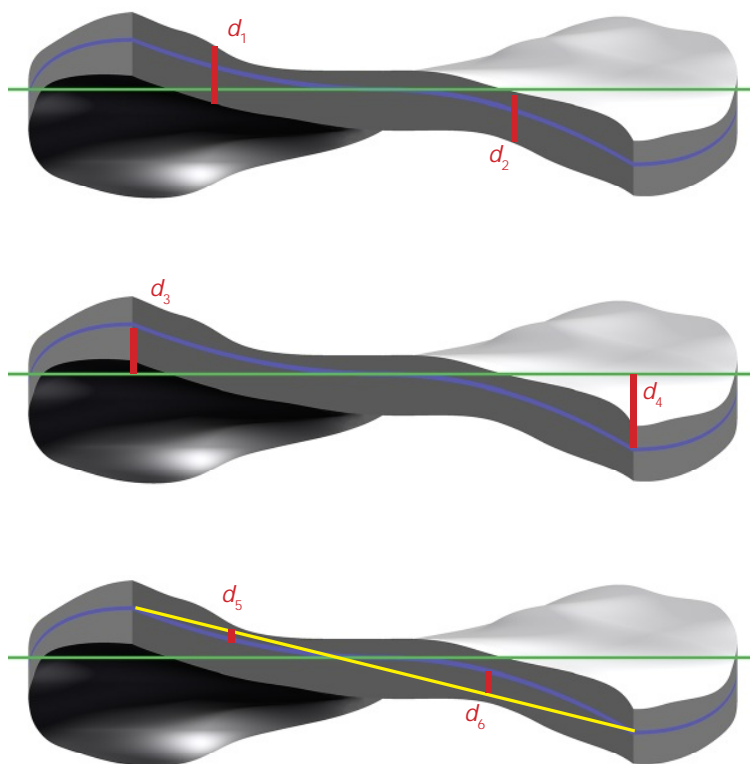


Fig. 22: Diagram of wafers with greatly exaggerated thickness inhomogeneity and curvature for the representation of size $d_1 \dots d_6$ from which the parameters of TTV, bow and warp are derived.

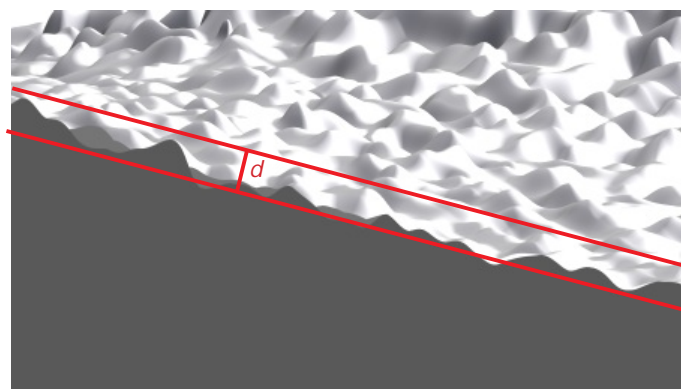


Fig. 23: The polishing process during the wafer production creates a very smooth surface with a roughness of 1 nm or better.

Micro-roughness

Irrespective of the thickness inhomogeneity which is expressed in the cm scale over the wafer in the variable TTV, there is a roughness on a substantially smaller μm and nm scale, which originates in the polishing step during the wafer production.

The (*Root Mean Square*, RMS) denotes the standard height deviation of a surface scan on a wafer.

For polished wafer sides, the RMS is typically specified at $< 1 \text{ nm}$; technically feasible is also $< 0.5 \text{ nm}$ which corresponds to a smoothness on the atomic scale.

Our Photoresists: Application Areas and Compatibilities

| Recommended Applications ¹ | | Resist Family | Photoresists | Resist Film Thickness ² | Recommended Developers ³ | Recommended Re-movers ⁴ |
|---------------------------------------|---|---------------------------|--|--|--|--|
| Positive | Improved adhesion for wet etching, no focus on steep resist sidewalls | AZ [®] 1500 | AZ [®] 1505 AZ [®] 1512 HS AZ [®] 1514 H AZ [®] 1518 | ≈ 0.5 µm ≈ 1.0 - 1.5 µm ≈ 1.2 - 2.0 µm ≈ 1.5 - 2.5 µm | AZ [®] 351B, AZ [®] 326 MIF, AZ [®] 726 MIF, AZ [®] Developer | AZ [®] 100 Remover, TechniStrip [®] P1316 TechniStrip [®] P1331 |
| | | | AZ [®] 4533 AZ [®] 4562 | ≈ 3 - 5 µm ≈ 5 - 10 µm | AZ [®] 400K, AZ [®] 326 MIF, AZ [®] 726 MIF, AZ [®] 2026 MIF | |
| | | | AZ [®] P4110 AZ [®] P4330 AZ [®] P4620 AZ [®] P4903 | ≈ 1 - 2 µm ≈ 3 - 5 µm ≈ 6 - 20 µm ≈ 10 - 30 µm | AZ [®] 400K, AZ [®] 326 MIF, AZ [®] 726 MIF, AZ [®] 2026 MIF | |
| | | | AZ [®] PL 177 | AZ [®] PL 177 | ≈ 3 - 8 µm | |
| | Spray coating | AZ [®] 4999 | | ≈ 1 - 15 µm | AZ [®] 400K, AZ [®] 326 MIF, AZ [®] 726 MIF, AZ [®] 2026 MIF | |
| | Dip coating | MC Dip Coating Resist | | ≈ 2 - 15 µm | AZ [®] 351B, AZ [®] 400K, AZ [®] 326 MIF, AZ [®] 726 MIF, AZ [®] 2026 MIF | |
| | Steep resist sidewalls, high resolution and aspect ratio for e. g. dry etching or plating | AZ [®] ECI 3000 | AZ [®] ECI 3007 AZ [®] ECI 3012 AZ [®] ECI 3027 | ≈ 0.7 µm ≈ 1.0 - 1.5 µm ≈ 2 - 4 µm | AZ [®] 351B, AZ [®] 326 MIF, AZ [®] 726 MIF, AZ [®] Developer | |
| | | | AZ [®] 9245 AZ [®] 9260 | ≈ 3 - 6 µm ≈ 5 - 20 µm | AZ [®] 400K, AZ [®] 326 MIF, AZ [®] 726 MIF | |
| Positive (chem. amplified) | Steep resist sidewalls, high resolution and aspect ratio for e. g. dry etching or plating | AZ [®] XT | AZ [®] 701 MiR (14 cPs) AZ [®] 701 MiR (29 cPs) | ≈ 0.8 µm ≈ 2 - 3 µm | AZ [®] 351B, AZ [®] 326 MIF, AZ [®] 726 MIF, AZ [®] Developer | AZ [®] 100 Remover, TechniStrip [®] P1316 TechniStrip [®] P1331 |
| | | | AZ [®] 12 XT-20PL-05 AZ [®] 12 XT-20PL-10 AZ [®] 12 XT-20PL-20 AZ [®] 40 XT | ≈ 3 - 5 µm ≈ 6 - 10 µm ≈ 10 - 30 µm ≈ 15 - 50 µm | AZ [®] 400K, AZ [®] 326 MIF, AZ [®] 726 MIF | |
| Image Re-verseal | Elevated thermal softening point and undercut for lift-off applications | AZ [®] 5200 | AZ [®] 5209 AZ [®] 5214 | ≈ 1 µm ≈ 1 - 2 µm | AZ [®] 351B, AZ [®] 326 MIF, AZ [®] 726 MIF | TechniStrip [®] Micro D2 TechniStrip [®] P1316 TechniStrip [®] P1331 |
| | | TI | TI 35ESX TI xLift-X | ≈ 3 - 4 µm ≈ 4 - 8 µm | | |
| Negative (Cross-linking) | Negative resist sidewalls in combination with no thermal softening for lift-off application | AZ [®] nLOF 2000 | AZ [®] nLOF 2020 AZ [®] nLOF 2035 AZ [®] nLOF 2070 | ≈ 1.5 - 3 µm ≈ 3 - 5 µm ≈ 6 - 15 µm | AZ [®] 326 MIF, AZ [®] 726 MIF, AZ [®] 2026 MIF | TechniStrip [®] NI555 TechniStrip [®] NF52 TechniStrip [®] MLO 07 |
| | | AZ [®] nLOF 5500 | AZ [®] nLOF 5510 | ≈ 0.7 - 1.5 µm | | |
| | Improved adhesion, steep resist sidewalls and high aspect ratios for e. g. dry etching or plating | AZ [®] nXT | AZ [®] 15 nXT (115 cPs) AZ [®] 15 nXT (450 cPs) | ≈ 2 - 3 µm ≈ 5 - 20 µm | AZ [®] 326 MIF, AZ [®] 726 MIF, AZ [®] 2026 MIF | TechniStrip [®] P1316 TechniStrip [®] P1331 TechniStrip [®] NF52 TechniStrip [®] MLO 07 |
| | | | AZ [®] 125 nXT | ≈ 20 - 100 µm | AZ [®] 326 MIF, AZ [®] 726 MIF, AZ [®] 2026 MIF | |

¹ In general, almost all resists can be used for almost any application. However, the special properties of each resist family makes them specially suited for certain fields of application.

² Resist film thickness achievable and processable with standard equipment under standard conditions. Some resists can be diluted for lower film thicknesses; with additional effort also thicker resist films can be achieved and processed.

³ Metal ion free (MIF) developers are significantly more expensive, and reasonable if metal ion free development is required.

Our Developers: Application Areas and Compatibilities

Inorganic Developers

(typical demand under standard conditions approx. 20 L developer per L photoresist)

AZ[®] Developer is based on sodium phosphate and –metasilicate, is optimized for minimal aluminum attack and is typically used diluted 1 : 1 in DI water for high contrast or undiluted for high development rates. The dark erosion of this developer is slightly higher compared to other developers.

AZ[®] 351B is based on buffered NaOH and typically used diluted 1 : 4 with water, for thick resists up to 1 : 3 if a lower contrast can be tolerated.

AZ[®] 400K is based on buffered KOH and typically used diluted 1 : 4 with water, for thick resists up to 1 : 3 if a lower contrast can be tolerated.

AZ[®] 303 specifically for the AZ[®] 111 XFS photoresist based on KOH / NaOH is typically diluted 1 : 3 - 1 : 7 with water, depending on whether a high development rate, or a high contrast is required

Metal Ion Free (TMAH-based) Developers

(typical demand under standard conditions approx. 5 - 10 L developer concentrate per L photoresist)

AZ[®] 326 MIF is 2.38 % TMAH- (TetraMethylAmmoniumHydroxide) in water.

AZ® 726 MIF is 2.38 % TMAH- (TetraMethylAmmoniumHydroxide) in water, with additional surfactants for rapid and uniform wetting of the substrate (e. g. for puddle development)

AZ® 826 MIF is 2.38 % TMAH- (TetraMethylAmmoniumHydroxide) in water, with additional surfactants for rapid and uniform wetting of the substrate (e. g. for puddle development) and other additives for the removal of poorly soluble resist components (residues with specific resist families), however at the expense of a slightly higher dark erosion.

Our Removers: Application Areas and Compatibilities

AZ® 100 Remover is an amine solvent mixture and standard remover for AZ® and T1 photoresists. To improve its performance, AZ® 100 remover can be heated to 60 - 80°C. Because the AZ® 100 Remover reacts highly alkaline with water, it is suitable for this with respect to sensitive substrate materials such as Cu, Al or ITO only if contamination with water can be ruled out..

TechniStrip® P1316 is a remover with very strong stripping power for Novolak-based resists (including all AZ® positive resists), epoxy-based coatings, polyimides and dry films. At typical application temperatures around 75°C, TechniStrip® P1316 may dissolve cross-linked resists without residue also, e.g. through dry etching or ion implantation. TechniStrip® P1316 can also be used in spraying processes. For alkaline sensitive materials, TechniStrip® P1331 would be an alternative to the P1316. Not compatible with Au.

TechniStrip® P1331 can be an alternative for TechniStrip® P1316 in case of alkaline sensitive materials. TechniStrip® P1331 is not compatible with Au.

TechniStrip® NI555 is a stripper with very strong dissolving power for Novolak-based negative resists such as the AZ® 15 nXT and AZ® nLOF 2000 series and very thick positive resists such as the AZ® 40 XT. TechniStrip® NI555 was developed not only to peel cross-linked resists, but also to dissolve them without residues. This prevents contamination of the basin and filter by resist particles and skins, as can occur with standard strippers. TechniStrip® NI555 is not compatible with GaAs.

TechniClean™ CA25 is a semi-aqueous proprietary blend formulated to address post etch residue (PER) removal for all interconnect and technology nodes. Extremely efficient at quickly and selectively removing organo-metal oxides from Al, Cu, Ti, TiN, W and Ni.

TechniStrip™ NF52 is a highly effective remover for negative resists (liquid resists as well as dry films). The intrinsic nature of the additives and solvent make the blend totally compatible with metals used throughout the BEOL interconnects to WLP bumping applications.

TechniStrip™ Micro D2 is a versatile stripper dedicated to address resin lift-off and dissolution on negative and positive tone resist. The organic mixture blend has the particularity to offer high metal and material compatibility allowing to be used on all stacks and particularly on fragile III/V substrates for instance.

TechniStrip™ MLO 07 is a highly efficient positive and negative tone photoresist remover used for IR, III/V, MEMS, Photonic, TSV mask, solder bumping and hard disk stripping applications. Developed to address high dissolution performance and high material compatibility on Cu, Al, Sn/Ag, Alumina and common organic substrates.

Our Wafers and their Specifications

Silicon-, Quartz-, Fused Silica and Glass Wafers

Silicon wafers are either produced via the Czochralski- (CZ-) or Float zone- (FZ-) method. The more expensive FZ wafers are primarily reasonable if very high-ohmic wafers (> 100 Ohm cm) are required.

Quartz wafers are made of monocrystalline SiO₂, main criterion is the crystal orientation (e. g. X-, Y-, Z-, AT- or ST-cut)

Fused silica wafers consist of amorphous SiO₂. The so-called JGS2 wafers have a high transmission in the range of ≈ 280 - 2000 nm wavelength, the more expensive JGS1 wafers at ≈ 220 - 1100 nm.

Our glass wafers, if not otherwise specified, are made of borosilicate glass.

Specifications

Common parameters for all wafers are diameter, thickness and surface (1- or 2-side polished). Fused silica wafers are made either of JGS1 or JGS2 material, for quartz wafers the crystal orientation needs to be defined. For silicon wafers, beside the crystal orientation (<100> or <111>) the doping (n- or p-type) as well as the resistivity (Ohm cm) are selection criteria.

Prime-, Test-, and Dummy Wafers

Silicon wafers usually come as „Prime-grade“ or „Test-grade“, latter mainly have a slightly broader particle specification. „Dummy-Wafers“ neither fulfill Prime- nor Test-grade for different possible reasons (e. g. very broad or missing specification of one or several parameters, reclaim wafers, no particle specification) but might be a cheap alternative for e. g. resist coating tests or equipment start-up.

Our Silicon-, Quartz-, Fused Silica and Glass Wafers

Our frequently updated wafer stock list can be found here: [⇒ www.microchemicals.com/products/wafers/waferlist.html](http://www.microchemicals.com/products/wafers/waferlist.html)

Further Products from our Portfolio

Plating

Plating solutions for e. g. gold, copper, nickel, tin or palladium: [⇒ www.microchemicals.com/products/electroplating.html](http://www.microchemicals.com/products/electroplating.html)

Solvents (MOS, VLSI, ULSI)

Acetone, isopropyl alcohol, MEK, DMSO, cyclopentanone, butylacetate, ... [⇒ www.microchemicals.com/products/solvents.html](http://www.microchemicals.com/products/solvents.html)

Acids and Bases (MOS, VLSI, ULSI)

Hydrochloric acid, sulphuric acid, nitric acid, KOH, TMAH, ... [⇒ www.microchemicals.com/products/etchants.html](http://www.microchemicals.com/products/etchants.html)

Etching Mixtures

for e. g. chromium, gold, silicon, copper, titanium, ... [⇒ www.microchemicals.com/products/etching_mixtures.html](http://www.microchemicals.com/products/etching_mixtures.html)

Further Information

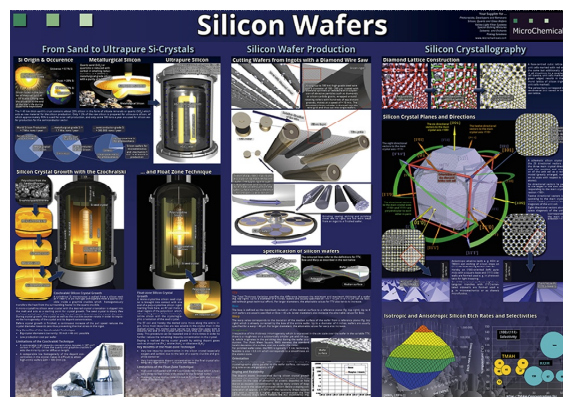
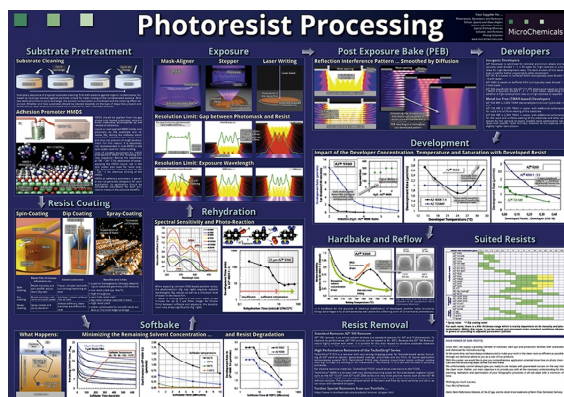
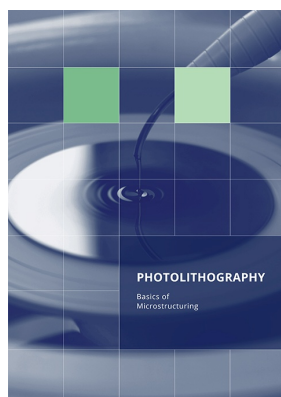
Technical Data Sheets:

www.microchemicals.com/downloads/product_data_sheets/photosresists.html

Material Safety Data Sheets (MSDS):

www.microchemicals.com/downloads/safety_data_sheets/msds_links.html

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